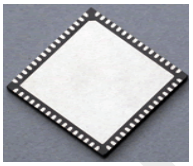
SPD1188 Datasheet

32-bit MCU with 14-bit ADC, 6 PGA's, 2 Buck DC/DC, integrated 3-phase Pre-Drivers with supply up to 96V

Features

- 32-bit ARM Cortex-M4 CPU Core with FPU
  - 200MHz maximum frequency
- Memories
  - 128 KB embedded flash
  - 512 bytes OTP flash
  - 64 KB on-chip SRAM
- Power Management
  - Integrated Buck DC/DC for pre-driver supply
  - Integrated Buck DC/DC for 3.3V supply
- Pre-Driver Module
  - 3-Phase Pre-Driver for BLDC motor control application with 96V max input voltage
  - Integrated bootstrap diodes
  - Integrated charge pump for 100% duty cycle
  - 2A and 1A pull-up and pull-down options
  - Programmable output swing from 9V to 18V
  - Six external power FET V_{DS} monitors
- Clock, reset and supply management
  - Brown-out Detect (BOD) on each power rail
  - Power-On Reset (POR)
  - 1 to 66 MHz external crystal oscillator
  - 32 MHz factory-trimmed RC oscillator
  - PLL for CPU clock
  - Typical 2.2MHz safety clock
- 14-bit A/D converters
  - As low as 140 ns conversion time
  - Conversion range: 0 to 3.65 V
  - Differential sampler
  - Triple-sample and hold capability
  - Open/short detection for safety
  - Temperature sensor



QFN40 (6 x 6 mm, 0.5mm pitch)
QFN56 (7 x 7 mm, 0.4mm pitch)

- Programmable gain amplifier (PGA)
  - Three integrated PGAs in MCU
  - Programmable Gains
    Single-ended: 1,2,4,8,12,16,24,32
    Differential: 2,4,8,16,24,32,48,64
  - Typical 400 ns settling time
- Motor PGA
  - Three differential PGAs with negative input voltage capability in Pre-Driver
  - Programmable Gains
    Differential: 2, 4, 8, 12, 16, 32, 64
  - Typical 400 ns settling time
- Analog comparator
  - Ten high-speed comparators
  - Output with digital deglitch filter
  - 4 DACs as reference
  - Optional DAC output buffer
  - Out of range voltage protection
  - Phase comparison
- PWM
  - Six enhanced PWM modules
  - 12 PWM outputs in total
  - Signal generation with phase lead/lag control
  - All events can trigger ADC conversion
- Up to 21 GPIO Pins
  - Configurable pull-up/pull-down resistors
  - Programmable digital input deglitch filter

- Enhanced Capture Module (ECAP)
  - Flexible input capture pin
  - Four 32-bit capture registers
  - Capture and PWM mode selection
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- 6 Timers
  - Three 32-bit general-purpose timers
  - Two 32-bit watchdog timers
  - SysTick timer 24-bit down-counter
- Communication interfaces
  - UART x 1, SPI x 1, I^2C x 1
- Deep sleep mode with off current as low as 15uA
- Security Modules
  - CRC x 1, AES x 1, 64-bit unique ID
- Operating temperature
  - Junction temperature: -40 to +125 °C
  - Ambient temperature: -40 to +105 °C

Peripheral	SPD1188API56	SPD1188ZAPI56	SPD1188YAPI56	SPD1188XAPI56	SPD1188WAPI56	SPD1188VAPI56	SPD1188API40
Flash (KB)	128	64	32	128	64	32	128
SRAM (KB)	64	32	16	64	32	16	64
OTP Flash(Bytes)	512						
GPIOs[1]	21						9
14-bit ADC Number of channels	1 10						1 5
PGA	3						
Analog comparators	8						5
DAC	4						
PWM Number of channels	6 12 channels						1 2 channels
ECAP	1						
General-purpose timers	3						
Watchdog timers	2						
AES	1						
CRC	1						
UART	1						
SPI	1						
I2C	1						
Maximum CPU frequency	200MHz	200MHz	200MHz	100MHz	100MHz	100MHz	200MHz

[1] Not including GPIO40 (BOOT) pin.

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Revision history

Version	Date	Author	Status	Changes
1	2019-02-11	H. Huang	Outdated	1. Initial release.
2	2019-04-12	H. Huang	Outdated	1. Modifies Table 3-1: SPD1188 QFN56 pin definitions. 2. Modifies Figure 1-3: Typical application diagram. 3. Modifies Figure 3-1: SPD1188 QFN56 pin-out. 4. Modifies Figure 6-1: Simplified Pre-Driver Board Schematic.
3	2019-08-16	H. Huang	Outdated	1. Modifies JTAG pin descriptions in Table 3-1: SPD1188 QFN56 pin definitions.
4	2019-09-30	H. Huang	Outdated	1. Modifies Figure 1-1: SPD1188 functional block diagram, change PWMTZ0/1 to EPWRTZ0/1. 2. Modifies Figure 1-3: Typical application diagram, update chip pin name.
5	2019-12-20	H. Huang	Outdated	1. Add Figure 1-2: Physical connection scheme between MCU and High voltage power module. 2. Extract content of Motor PGA from Section 2.17 PGAs and add a new section for Motor PGA. 3. Update Figure 2-2: Typical application diagram for Motor PGA. 4. Update Table 3-1: SPD1188 QFN56 pin definitions, modify descriptions of PGA_P_U and PGA_N_U. 5. Add Table 3-3: PGA input channel selection. 6. Add Table 5-19: ESD absolute maximum ratings. 7. Add Table 5-20: Electrical sensitivities.
6	2020-03-11	H. Huang	Outdated	1. Update Section 2.8, add safety clock description. 2. Update Section 2.9 for boot mode description.
7	2020-05-30	H. Huang	Outdated	1. Update Figure 1-1: SPD1188 functional block diagram. 2. Update Figure 1-2: Physical connection scheme between MCU and High voltage power module. 3. Update Section 2.9 for boot mode description. 4. Update Section 2.14 and modify the maximum speed of SPI. 5. Update Section 2.19 for phase comparison.

Version	Date	Author	Status	Changes
				6. Update Table 5-3: I/O Electrical characteristics. 7. Update Table 5-7: Internal 1.2V regulator characteristics. 8. Update Figure 5-2: Internal 1.2V regulator load regulation. 9. Add Table 5-8: BOD characteristics. 10. Add Table 5-9: RCO characteristics. 11. Add Table 5-10: PLL characteristics. 12. Add Table 5-11: XO characteristics. 13. Update Table 5-12: ADC characteristics. 14. Add Chapter 8 for ordering information. 15. Add Table 5-24: SPI characteristics.
8	2020-07-31	H. Huang	Outdated	1. Update Section 2.12 for UART features. 2. Add Figure 5-3: Internal 1.2V regulator load regulation with different temperature. 3. Update Table 5-13: PGA characteristics. 4. Update Table 5-18: Flash memory characteristics.
9	2021-03-28	H. Huang	Outdated	1. Update Table 5-3: I/O Electrical characteristics. 2. Add characteristics of ambient temperature T_A. 3. Update Table 8-1: Ordering information. 4. Update Section 2.12 for UART features. 5. Update Table 5-13: PGA characteristics. 6. Add Figure 7-2: QFN56 – 56 pin, 7mm x 7mm quad flat no-lead recommended footprint. 7. Update comparator pin descriptions in Table 3-1: SPD1188 QFN56 pin definitions. 8. Add Table 3-4: GPIO pin function and state after reset. 9. Add note for Table 5-4: SPD1188 typical current consumption (Run in FLASH). 10. Add note for Table 5-5: SPD1188 typical current consumption (Run in RAM). 11. Update Table 5-6: Peripheral current consumption. 12. Update Table 5-20: Electrical sensitivities. 13. Update Figure 3-1: SPD1188 QFN56 pin-out and its notes.
10	2021-12-01	H. Huang	Outdated	1. Add Table 5-21: Moisture sensitivity characteristic. 2. Update typical and maximum value of VDDG.

Version	Date	Author	Status	Changes
				3. Update Table 3-3: PGA input channel selection. 4. Update Table 5-15: Comparator characteristics. 5. Add Figure 5-4: The negative resistance of the on-chip crystal oscillator at 50 . 6. Add Figure 5-5: The negative resistance of the on-chip crystal oscillator at 85 . 7. Add Figure 5-6: The negative resistance of the on-chip crystal oscillator at 100 . 8. Add Figure 5-7: The negative resistance of the on-chip crystal oscillator at 125 . 9. Update Table 3-1: SPD1188 QFN56 pin definitions, modify the description for debug pins. 10. Update Table 5-4: SPD1188 typical current consumption (Run in FLASH). 11. Update Table 5-5: SPD1188 typical current consumption (Run in RAM). 12. Update Figure 5-1: Typical operational current versus frequency.
11	2022-07-08	H. Huang	Outdated	1. Update Section 2.22. 2. Update Table 5-3: I/O Electrical characteristics, remove parameter I_{OZ}. 3. Update Chapter 6. 4. Update Table 5-14: Motor PGA characteristics. 5. Update Section 2.9 and Section 2.10. 6. Update Conditions of parameter R_{PU} and R_{PD} in Table 5-3: I/O Electrical characteristics. 7. Update Table 3-3: PGA input channel selection.
12	2022-08-22	H. Huang	Outdated	1. Update Table 8-1: Ordering information, change ordering number.
A/0	2022-10-24	H. Huang	Outdated	1. Update document format. 2. Add information for QFN40 package.
C/0	2025-07-29	J. Zhou	Outdated	1. Update the document template. 2. Add thermal resistance characteristics. 3. Add the performance description of the waveforms generated by the DAC. 4. Modify the minimum values of VBAT and VDDG to 9 V. 5. Update f_{RCO} in Table 5-9.
C/1	2025-08-05	J. Zhou	Outdated	1. Update f_{RCO} in Table 5-9.
C/2	2025-08-12	J. Zhou	Outdated	1. Update f_{RCO} in Table 5-9.
C/3	2025-11-05	J. Zhou	Outdated	1. Correct the number of peripherals.

Version	Date	Author	Status	Changes
C/4	2026-06-30	J. Zhou	Outdated	1. Update the functional description of the pre-programmed IO module. 2. Add Important Statement and Disclaimer. 3. Add Figure 2-1 in Section 2.8. 4. Modify the packaging of SPD1188API40 in Table 8-1 to reel, and add Section 7.2.2.
C/5	2026-08-05	J. Zhou	Released	1. Delete pre-programmed IO module (SIO).

Terms or abbreviations

Terms or abbreviations	Description
MCU	Microcontroller Unit
SWD	Serial Wire Debug
AHB	Advanced High Performance Bus
XIP	Execution In Place
PLL	Phase Locked Loop
BOD	Brownout Detector
PFD	Phase Frequency Detector
NVIC	Nested Vectored Interrupt Controller
UART	Universal Asynchronous Receiver-Transmitter
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
PGA	Programmable-Gain Amplifier
CRC	Cyclic Redundancy Check
AES	Advanced Encryption Standard

1 Device overview

SPD1188 is a SiP (System in a Package) device integrating MCU, Pre-Driver module and power management module to have “all-in-one” chip for BLDC motor driving application with supply voltage up to 96V.

The MCU incorporates a 32-bit ARM Cortex-M4 high-performance processor with a software-programmable clock rate as high as 200 MHz, 64 KB SRAM, embedded flash with 128 KB, and an extensive range of enhanced I/Os and peripherals. The device offers a 14-bit ADC, six PGAs, six enhanced PWMs, three general purpose 32-bit timers, as well as standard and advanced communication interface: an UART, an I^2C and a SPI. These features make the SPD1188 ideal for motor control application.

The Pre-Driver module provides three half-bridge pre-drivers, with programmable charging/ discharging current capability up to 2A. Integrated Charge Pump supports 100% duty cycle.

The Power management module includes a 96V Max input, 12V 300mA output synchronous HV buck, a 12V input, 3.3V 500mA output synchronous LV buck, and Brown-out-Detection observing each of the power rail.

The temperature range is from -40 °C to +125 °C. The package type is 56-pin or 40-pin QFN.

Figure 1-1 shows the functional block diagram for the SPD1188. The physical connection scheme between the MCU and the high voltage power module is show in Figure 1-2. The typical application diagram is shown in Figure 1-3.

Figure 1-1: SPD1188 functional block diagram

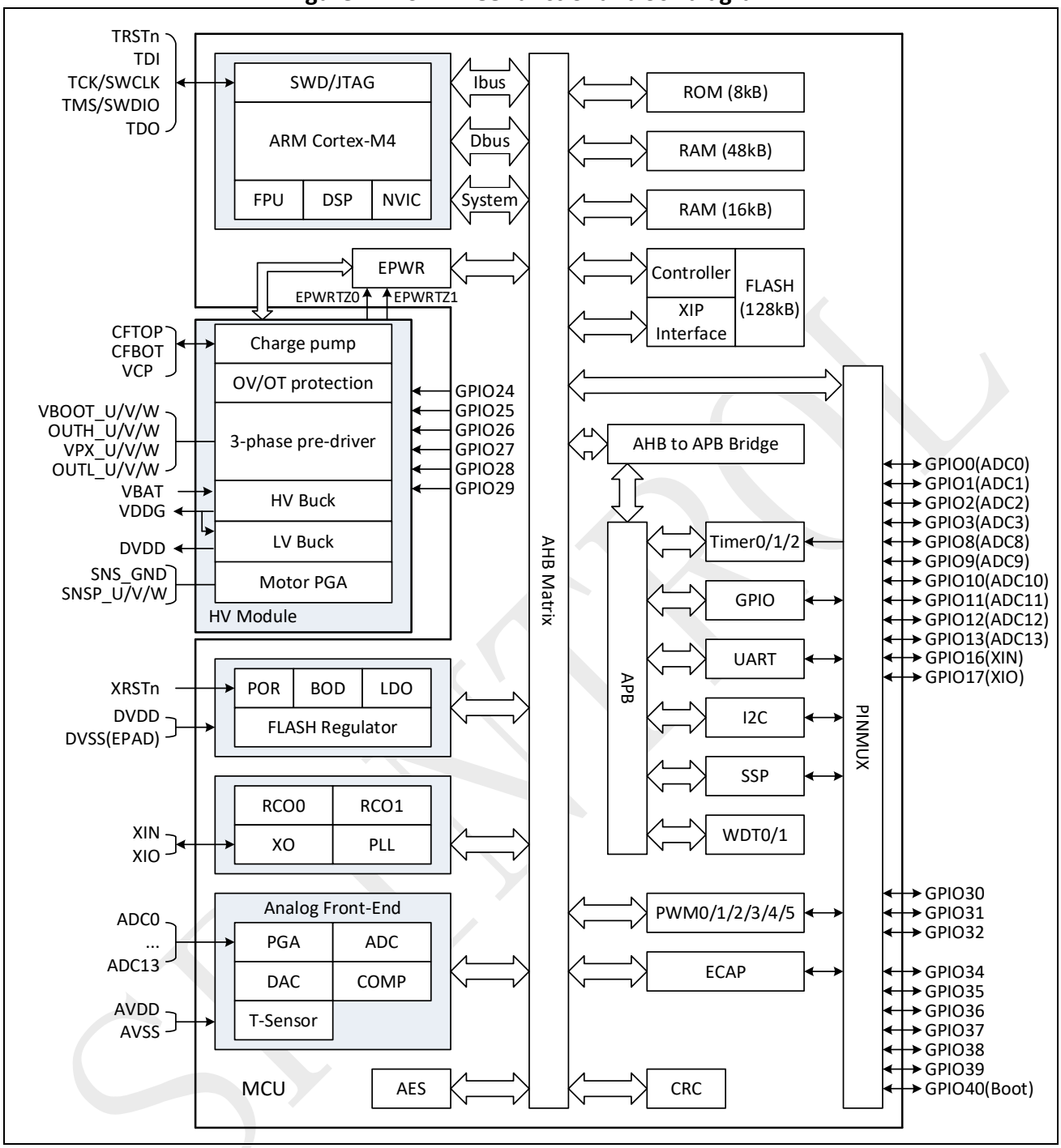


Figure 1-2: Physical connection scheme between MCU and High voltage power module

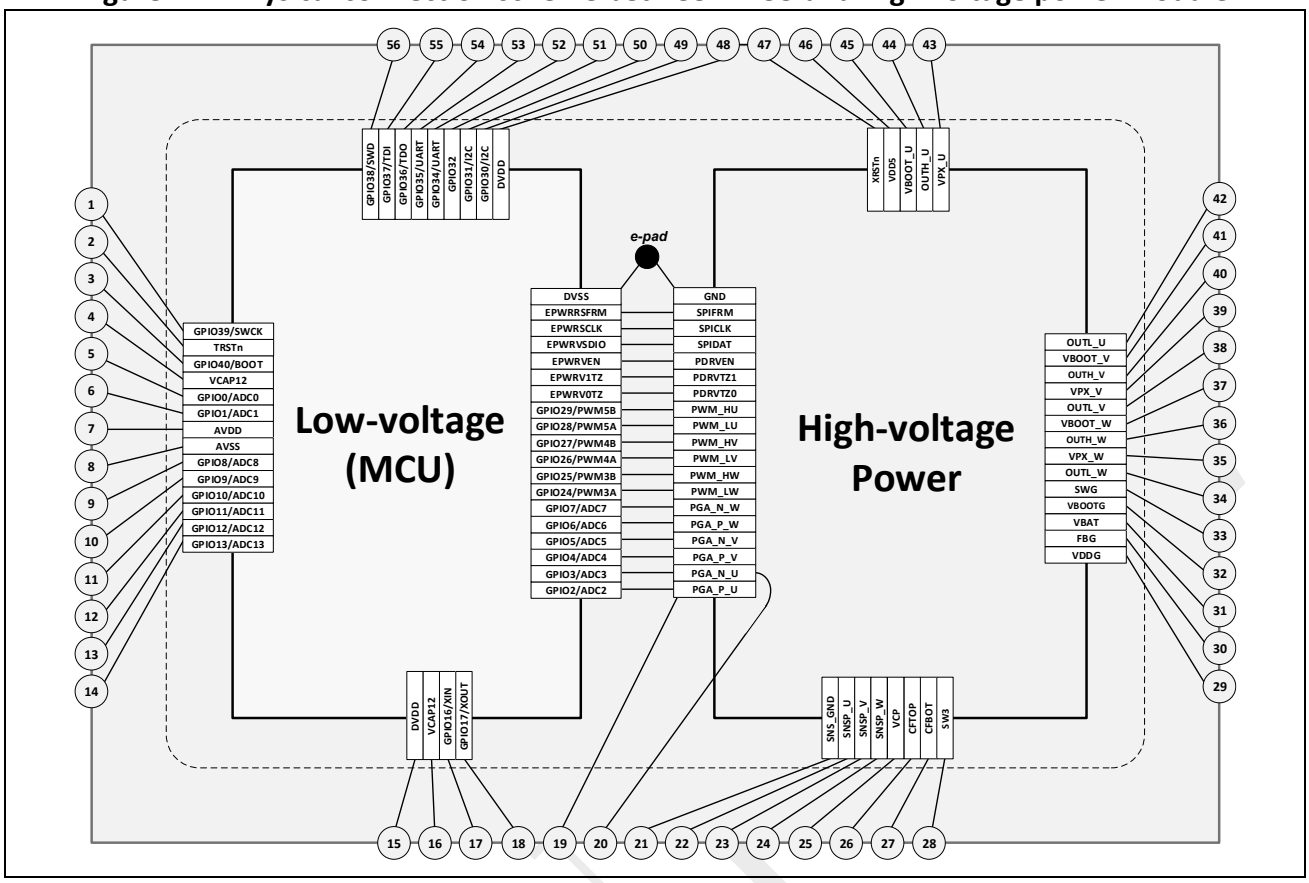
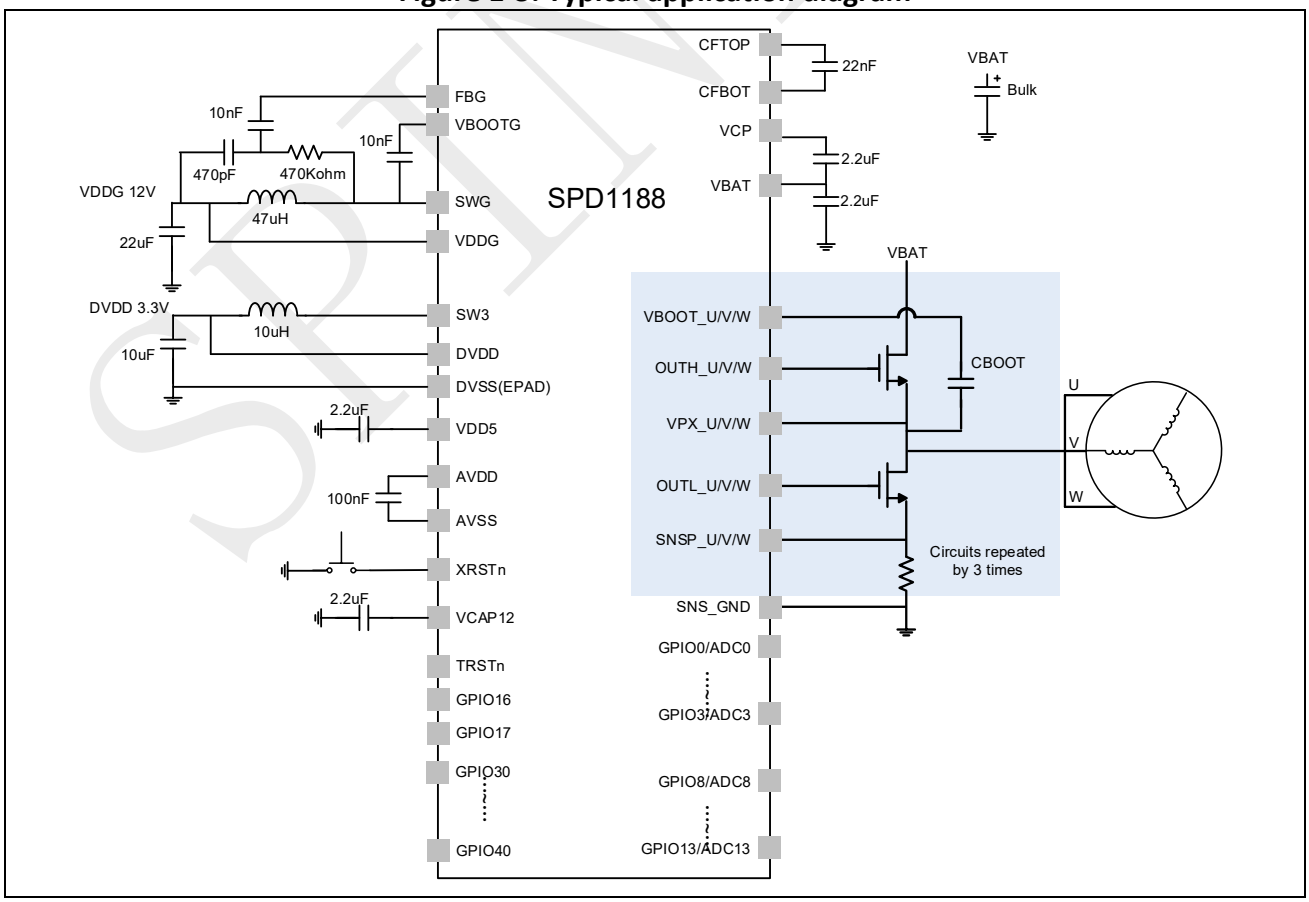


Figure 1-3: Typical application diagram



2 Feature descriptions

2.1 ARM Cortex-M4 core

The ARM Cortex-M4 processor has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The SPD1188 integrates a full-feature ARM Cortex-M4 core with FPU that can run up to 200MHz. Therefore, it is compatible with all ARM tools and software.

2.2 Embedded SRAM

The SPD1188 has implemented 64 KB SRAM memory for code and data. The SRAM can be accessed (read/write) at CPU clock speed with 0 wait states.

2.3 Embedded Flash memory

Up to 128 KB of embedded Flash memory is available for storing programs and data.

2.4 Nested vectored interrupt controller (NVIC)

The SPD1188 embeds a nested vectored interrupt controller able to handle up to 51 mask-able interrupt channels (not including the 16 interrupt lines of Cortex-M4) and 16 programmable priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Support for lazy-stacking
- Interrupt entry restored on interrupt exit with no instruction overhead

2.5 External interrupt/event controller

The SPD1188 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. In addition, any GPIO interrupt can be configured as edge-triggered or level-triggered.

2.6 Power supply, reset and deep sleep mode

The SPD1188 requires a single 9V to 96V power supply. All derivative supplies such as low-side pre-driver supply, main digital MCU 3.3V supply, MCU 1.2V supply are generated on-chip from a single input supply. External generation option for derivative supplies is also available.

The SPD1188 has a global reset pin as well as an integrated power-on reset (POR) circuitry. The POR circuitry guarantees all power-up reset sequence requirements and makes the device easy to use.

Deep sleep mode option is provided, during which, both HV buck and LV buck will be disabled and all the control blocks are disabled except reset monitoring logics used to wait for wake-up command. So, the turn off current can be as low as 15uA.

2.7 Brown-out detector

The device features an embedded brown-out detector (BOD) that monitors the main input supply V_{BAT}, low-side pre-driver supply V_{DDG}, main digital MCU 3.3V supply V_{DD} and MCU 1.2V supply voltage levels and compare them to the programmable pre-set values. An interrupt or reset can be generated when voltage of any of the power domains is higher or lower their respective pre-set values. The interrupt service routine will then generate a warning message and/or put the MCU into a safe state. The BOD is enabled by software. The MCU BOD for 3.3/1.2V supplies is implemented inside the MCU, separately from high-voltage BOD system.

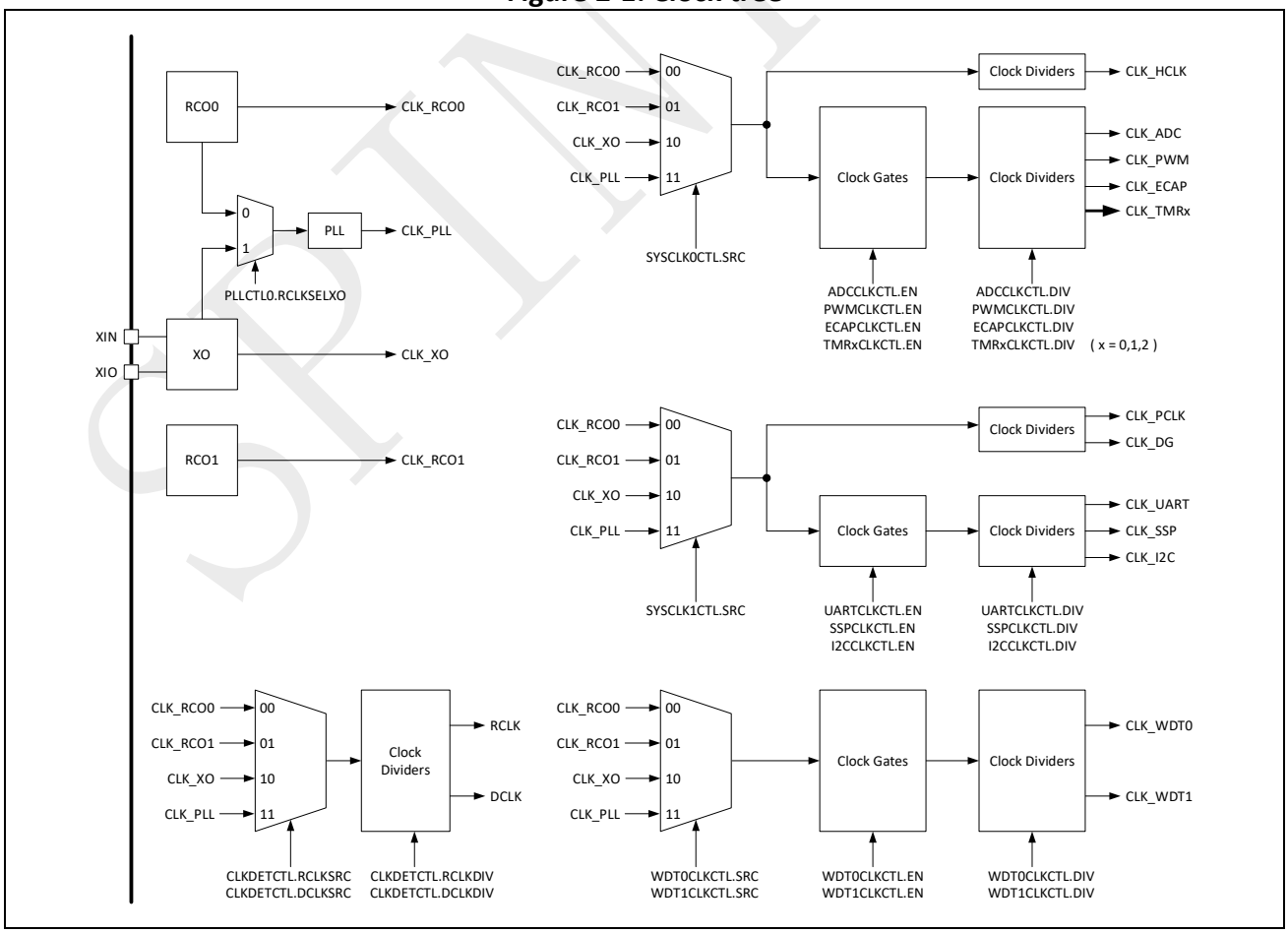
2.8 Clocks

The MCU system clock selection is performed on startup. The internal 32 MHz RC oscillator is selected by default upon reset. An external 1 – 66 MHz oscillator can be selected by the user.

The device implements a fractional phase-lock loop (PLL) for high frequency clock generation. The PLL can take the internal RC oscillator or external clock as the input reference clock. The output frequency covers range from 25MHz to 200MHz.

Several clock dividers allow the configuration of the AHB, APB and the peripherals frequency. The maximum allowed frequency is 200MHz for AHB and 50 MHz for APB. See Figure 2-1 for details on the clock tree. Special clock selection logic is designed so that the backup clock can take charge if current clock is missing. The 2.2MHz backup-safety oscillator makes the SPD1188 get rid of clock stuck.

Figure 2-1: Clock tree



2.9 Boot mode

The boot code is located in on-chip ROM memory. After reset, the ARM processor starts code execution from the ROM. The boot pin and TRSTn pin are used to select one of the two boot options:

- Boot from embedded Flash (boot pin = 1, TRSTn pin = X): the boot loader jumps to the embedded Flash and runs from the address at 0x1000 0000
- ISP mode (boot pin = 0, TRSTn pin = 0): the boot loader reprograms the embedded Flash by using UART. During the process, the GPIO34 is configured as UART_TXD and the GPIO35 is configured as UART_RXD.

Note: The boot pin should always keep high when chip normally running.
The TRSTn pin is recommended to set as low.
When TRSTn is high, the related debug interface pins (GPIO36 ~ GPIO39) must not be used as GPIO function.

2.10 General-purpose IOs (GPIOs)

The SPD1188 can be configured to support as many as 21 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It features:

- Each GPIO pin has configurable internal pull-up and pull-down resistors
- Each GPIO pin has a programmable digital input deglitch filter

2.11 Timers and watchdogs

The SPD1188 device includes three general-purpose timers, two watchdog timers and a SysTick timer.

General-purpose timers

The SPD1188 includes three identical 32-bit general-purpose timers. Each general-purpose timer consists of a 32-bit auto-reload down-counter. An interrupt would be generated when the counter reaches zero if it is enabled. When the counter reaches zero, the timer can also generate an ADCSOC event or a PWMSYNC event if they are enabled. The clock of general-purpose timer can be selected from internal RC oscillators, external oscillator or PLL clock. Besides, each general-purpose timer can also capture external input as timer clock or enable signal.

Watchdogs

The SPD1188 implements two identical watchdogs. Each watchdog is based on a 32-bit down-counter, which can be clocked from internal RC oscillators, external oscillator or PLL clock. When the counter reaches the given time-out value, an interrupt or a reset can be generated. The watchdog counter can be frozen or free-running in debug mode.

SysTick Timer

This timer is dedicated for OS, but could also be used as a standard down-counter. It features:
- A 24-bit down-counter
- Auto-reload capability
- Mask-able system interrupt generation when the counter reaches 0

2.12 UART

The SPD1188 has an UART module. It features:
- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data
- 5 – 8 data bits
- Even, odd or no parity detection
- One, one-and-a-half, or two stop bits generation
- Baud-rate generation up to 12.5 Mbps
- 64-byte transmit FIFO
- 64-byte receive FIFO
- Auto baud-rate detection

2.13 I^2C

The I^2C bus interface features:
- Three speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s) and High-Speed mode (2 Mb/s)
- Clock synchronization
- Master or slave I^2C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 16 x 32-bit deep transmit and receive buffers, respectively

2.14 SPI

The SPI allows half/full-duplex, synchronous, serial communication with external devices. It features:
- Full-duplex synchronous transfers

- Master or slave operation
- 1 to 32-bit transfer frame format selection
- 50 Mbps maximum communication speed
- MSB-first data order
- Programmable clock polarity and phase
- Transmit and receive FIFOs

2.15 ADC

A 14-bit analog-to-digital converter is embedded into SPD1188 and has up to 8 channels. In addition, the temperature sensor, internal powers and PGA outputs can be selected as ADC input channels. These inputs are multiplexed internally. The ADC core has three independent built-in sample-and-hold (S/H) blocks. Each S/H has two input channels, which is suitable for differential sampling.

The events generated by the general-purpose timers and the PWM outputs can be internally connected to the ADC start trigger.

- 14-bit resolution
- 140 ns minimum conversion time and independent configurable sampling time
- Differential sampling
- Triple-sample and hold capability
- Simultaneous sampling and sequential sampling modes supported
- Full range analog input: 0 V to 3.65 V
- Reference voltage can be selected from internal or external source
- ADC external channel input open and short detection for safety

Please see Table 5-12 for ADC characteristics.

2.16 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. It is internally connected to the ADC input channel, which is used to convert the sensor output voltage into a digital value.

2.17 PGAs

Three flexible programmable gain amplifiers (PGAs) are embedded into MCU portion of SPD1188 and share up to 8 input channels. The temperature sensor and internal 1.2V power can be selected as a PGA input channels. These inputs are multiplexed. Each PGA outputs are connected to ADC input channel.

- Programmable gains for general purpose PGAs
  Differential mode: 2, 4, 8, 16, 24, 32, 48, 64; Single-ended mode: 1, 2, 4, 8, 12, 16, 24, 32.
- Differential mode optimized for motor current sensing using on-board resistive level shifters
  Settling time: 400 ns to 800 ns

Please see Table 5-13 for on-MCU PGA characteristics.

2.18 Motor PGAs

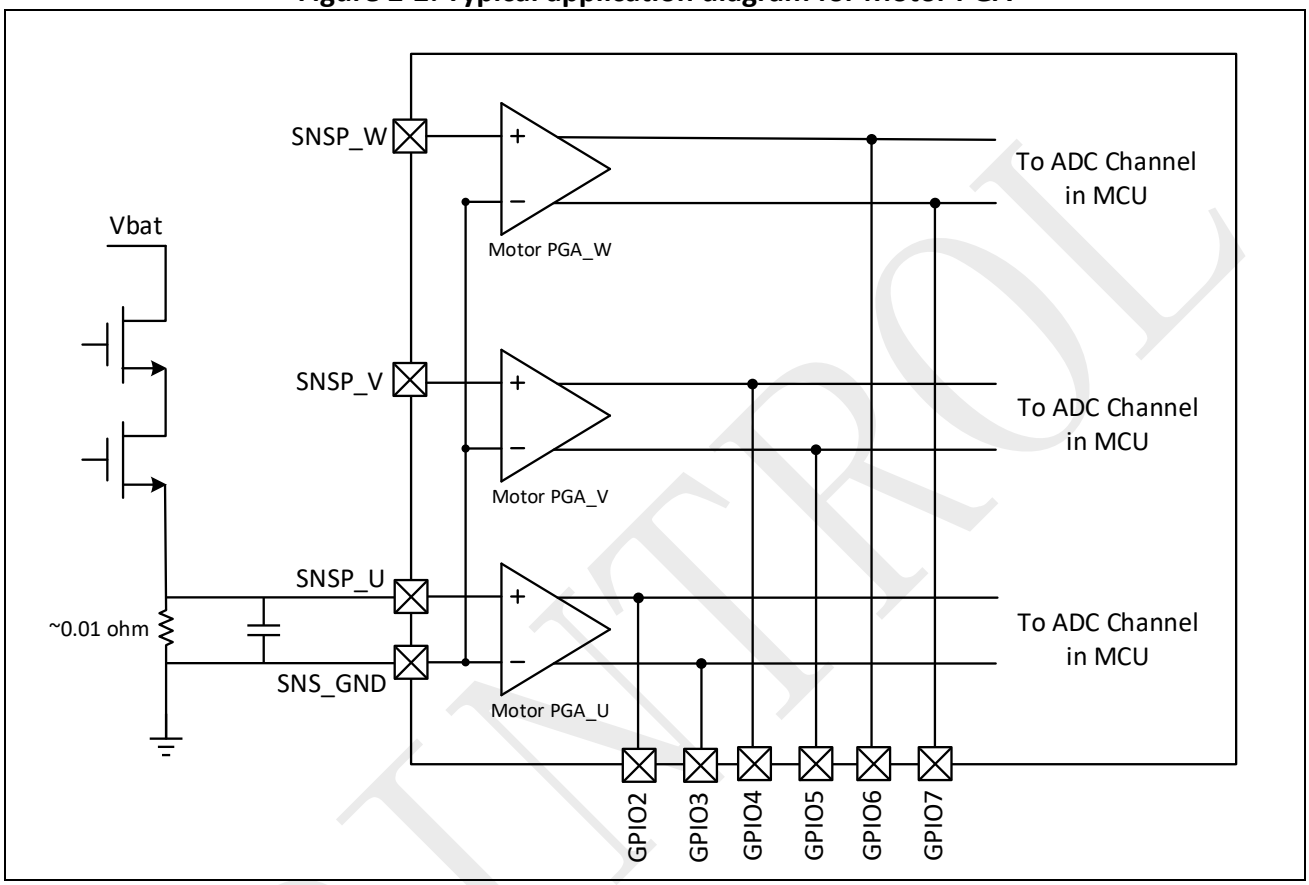
Additionally, three fully differential PGA's are provided in SPD1188 Pre-Driver module. These PGA's common mode voltage can be close to GND and thus suitable for direct motor current sensing without on-board resistive level shifter. Figure 2-2 shows the typical application diagram for motor PGA. Programmable gain is realized by selecting different feedback resistor Rf. The connection

relationship between Motor PGA and ADC channel is shown in Figure 1-2. **Due to the design scheme, when motor PGA is used, GPIO2 and GPIO3 has to be floating.**

- Programmable gains for Motor PGAs
  Differential mode: 2, 4, 8, 12, 16, 32, 64

Please see Table 5-14 for Motor PGA characteristics.

Figure 2-2: Typical application diagram for Motor PGA



2.19 Analog comparators

The SPD1188 has 8 high-speed comparators. Each comparator use the internal DAC as reference to monitor whether the PGA inputs or outputs exceed the threshold. A DAC can be used to generate a static voltage as a threshold for the somparator, but does not guarantee the performance of the waveform. Two comparators are designed for each PGA: one is monitoring whether the voltage is too high, the other is monitoring whether the voltage is too low. The extra two pairs of comparators are reserved for additional applications. The comparator output is routed to the PWM Trip-Zone modules. Additionally, each comparator can implement the phase comparison for motor commutation. The detail channel selection can be referred to Technical Reference Manual.

- 50 ns typical response
- Programmable hysteresis
- Output with digital deglitch filter
- Phase comparison

Please see Table 5-15 and Table 5-16 for analog comparator and DAC characteristics.

2.20 PWMs

The SPD1188 integrates 6 PWM modules and supports 12 PWM channels. Without much involvement of processor core, the PWMs can generate complex pulse width waveforms.

Each PWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Each PWM module can generate two outputs with single-edge operation, dual-edge symmetric operation or dual-edge asymmetric operation
- All events can trigger both CPU interrupts and ADC start of conversion
- Programmable phase-control support for lag or lead operation relative to other PWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions

2.21 ECAP

The enhanced capture (ECAP) module is essential in systems where accurate timing of external events is important. The SPD1188 has implemented an ECAP module with following features:

- Flexible input capture pin: each GPIO can be configured as capture pin
- 32-bit time base counter
- 4 x 32-bit time-stamp capture registers
- 4-stage sequencer that is synchronized to external events
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Interrupt capabilities on any of the 4 capture events

2.22 Cyclic redundancy check (CRC)

The SPD1188 has a hardware CRC calculation unit. The CRC module is used to verify data transmission or storage integrity. It features:

- 32-bit parallel bit stream input, and up to 32-bit CRC output
- Supports up to 2^{32} byte length for CRC calculation
- Five CRC standard polynomials supported

2.23 Advanced encryption standard (AES) engine

The AES engine provides fast hardware encryption and decryption services. The main features are as follows:

- Supports as many as six block cipher modes: ECB, CBC, CTR, CCM*, MMO, and Bypass
- Supports 128-, 192-, and 256-bits key size
- Error indication for each block cipher mode
- Separate 4 x 32-bit input and output FIFOs

2.24 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded and is a combined JTAG and serial wire debug port. The SWJ-DP interface enables either a serial wire debug or a JTAG probe to be connected to the target. The debug port can be disabled when enabling SPD1188 certain security feature.

2.25 Power management module

SPD1188 integrates power management module including HV Buck, LV Buck providing 10V and 3.3V power rail respectively.

HV buck converts main input supply V_{BAT} to V_{DDG} rail, which is typically 10V for defining pre-driver output voltage swing. HV buck uses synchronous rectification with no external power FET or diode. On-board compensation network is needed and the values of each passive component are shown in the typical application diagram in Figure 1-3. HV buck will start operating when V_{BAT} voltage is higher than 8.15V and shut down when V_{BAT} voltage drops below 7.65V. Typical switching frequency for HV buck is 600 kHz, and typical current limit value is 300mA.

LV buck converts V_{DDG} to DVDD rail, which is typically 3.3V for powering MCU. LV buck uses synchronous rectification with no external power FET or diode. No compensation network is needed. Inductor value is 10uH and output cap is 10uF as shown in the typical application diagram in Figure 1-3. LV buck will start operating when V_{DDG} voltage is higher than 6.5V and shut down when V_{VDDG} voltage drops below 6.2V. During power up, it will wait for HV buck to finish soft start, typically 1ms, before start operating. Typical switching frequency for LV buck is 1.2MHz, and typical current limit value is 600mA.

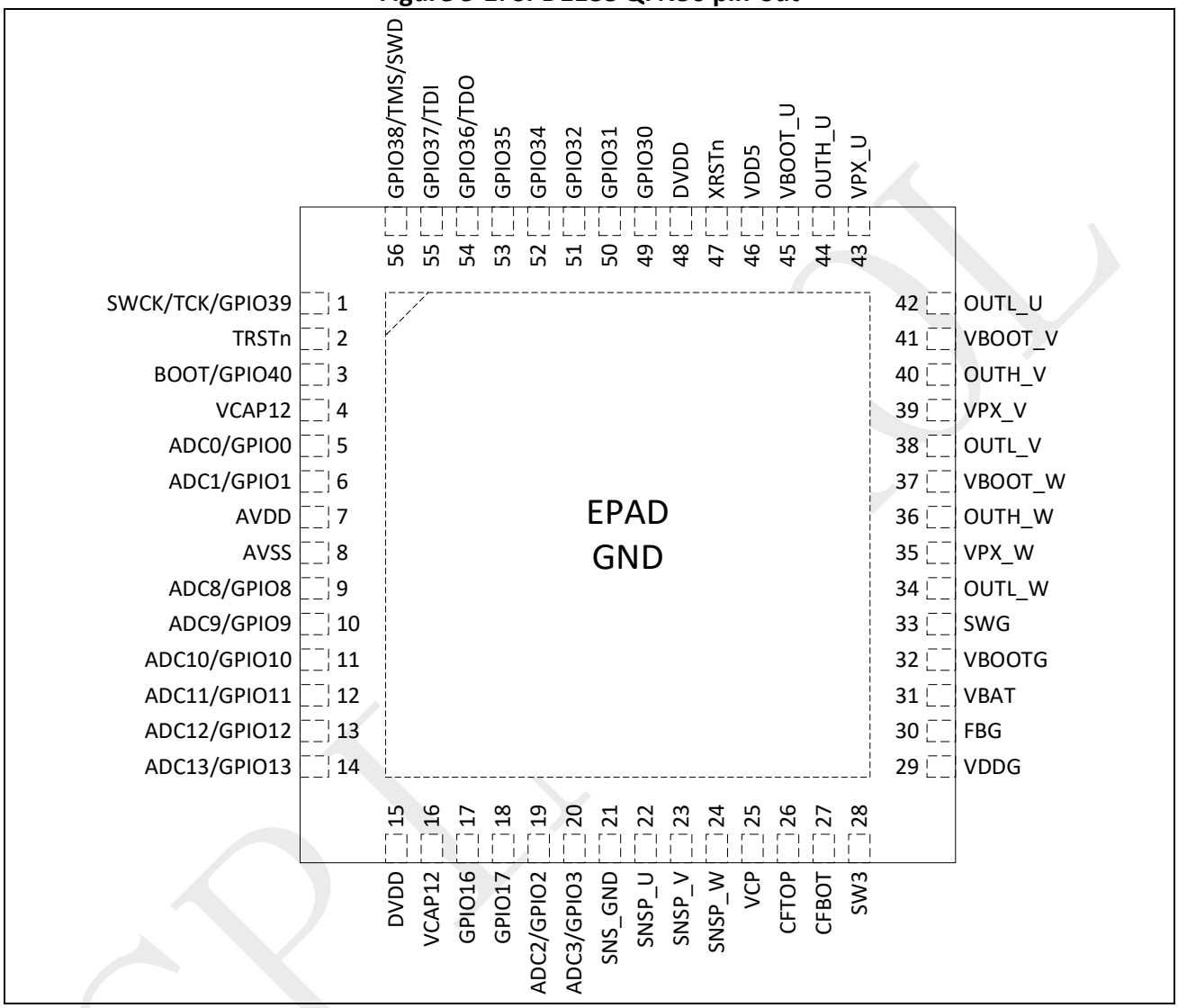
2.26 Pre-Driver system

Pre-driver system consists of a three low- and high-side pre-drivers which can drive the three phases of low- and high-side external power NFET's or IGBT's. The voltage range of each low-side pre-driver is zero to V_{DDG}, which is typically 10V. The embedded charge pump guarantees 100% duty cycle, i.e. allows high-side of each phase to be on indefinitely without loss of charge on the high-side pre-driver stage. Non-overlap time is built in to prevent high side and low side power FET to turn on at the same time even in case of overlapping input PWM command. VDS monitor is used to observe the Drain to Source voltage of the turned-on external power FET and compare it to pre-set programmable reference. When excessive current flows through the power FET, fault will be trigger to stop the Motor PWM signal through PWM trip zone.

3 Pinout and pin description

3.1 QFN56

Figure 3-1: SPD1188 QFN56 pin-out



[1] The above figure shows the package top view.

[2] **Note: there is no need to connect the two VCAP12 pins on the PCB boards**.

[3] **Note: when TRSTn is HIGH, GPIO36 ~ GPIO39 pins work as Debug interface and can't be configured as other functions**.

Table 3-1: SPD1188 QFN56 pin definitions

Pin	Signal	Type[1]	Description
1	GPIO39	I/O	General-purpose input/output 39
	TCK/SWCK	I	JTAG clock or SWD clock
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	PWM2B	O	PWM2 output B
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
2	TRSTn	I	JTAG reset pin, reset the JTAG when low
3	BOOT(GPIO40)	I/O	Boot pin (General-purpose input/output 40)
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZ0O	O	Trip-zone signal 0 from ePower module for monitoring
	EPWRTZ1O	O	Trip-zone signal 1 from ePower module for monitoring
4	VCAP12	S	1.2V power
5	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
6	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
7	AVDD	S	Analog power
8	AVSS	S	Analog ground
9	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
	SPI_SCLK	I/O	SPI clock input/output
	COMP3H	O	Comparator COMP3H result output
	PWMSOC	O	PWM SOC signal output for monitoring
10	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
	SPI_SFRM	I/O	SPI frame signal
	COMP3L	O	Comparator COMP3L result output
11	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	COMP4H	O	Comparator COMP4H result output
12	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	COMP4L	O	Comparator COMP4L result output
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZO[2]	O	Trip-zone signal from ePower module for monitoring

Pin	Signal	Type[1]	Description
13	GPIO12	I/O	General-purpose input/output 12
	ADC12	AI	ADC channel 12 input
	I2C_SCL	I/O	I^2C clock
14	GPIO13	I/O	General-purpose input/output 13
	ADC13	AI	ADC channel 13 input
	I2C_SDA	I/O	I^2C data
15	DVDD	S	Digital power
16	VCAP12	S	1.2V power
17	GPIO16	I/O	General-purpose input/output 16
	XIN	AI	External oscillator input
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWM2A	O	PWM2 output A
	PWM5A	O	PWM5 output A
18	GPIO17	I/O	General-purpose input/output 17
	XIO	AI/O	External oscillator input/output
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	PWM2B	O	PWM2 output B
	PWM5B	O	PWM5 output B
19	GPIO2	I/O	General-purpose input/output 2
	ADC2/PGA_P_U	AI/O	ADC channel 2 input or U phase Motor PGA positive output, **when Motor PGA is enabled, GPIO2 and GPIO3 has to be floating**
	COMP1H	O	Comparator COMP1H result output
20	GPIO3	I/O	General-purpose input/output 3
	ADC3/PGA_N_U	AI/O	ADC channel 3 input or U phase Motor PGA negative output, **when Motor PGA is enabled, GPIO2 and GPIO3 has to be floating**
	COMP1L	O	Comparator COMP1L result output
21	SNS_GND	AI	Ground sense for Motor PGA
22	SNSP_U	AI	U Phase current sense for Motor PGA
23	SNSP_V	AI	V Phase current sense for Motor PGA
24	SNSP_W	AI	W Phase current sense for Motor PGA
25	VCP	S	Charge pump output
28	CFTOP	S	Charge Pump Flying Capacitor Top Plate Voltage
27	CFBOT	S	Charge Pump Flying Capacitor Bottom Plate Voltage
28	SW3	S	LV buck switching pin
29	VDDG	S	V_{DDG} supply pin
30	FBG	AI	HV buck Feedback pin
31	VBAT	S	VBAT supply pin
32	VBOOTG	S	HV buck bootstrap pin
33	SWG	S	HV buck switching pin
34	OUTL_W	O	Pre-Driver W-Phase Low Side FET Gate Drive
35	VPX_W	O	Pre-Driver W-Phase Power FET Switching Node
36	OUTH_W	O	Pre-Driver W-Phase High Side FET Gate Drive

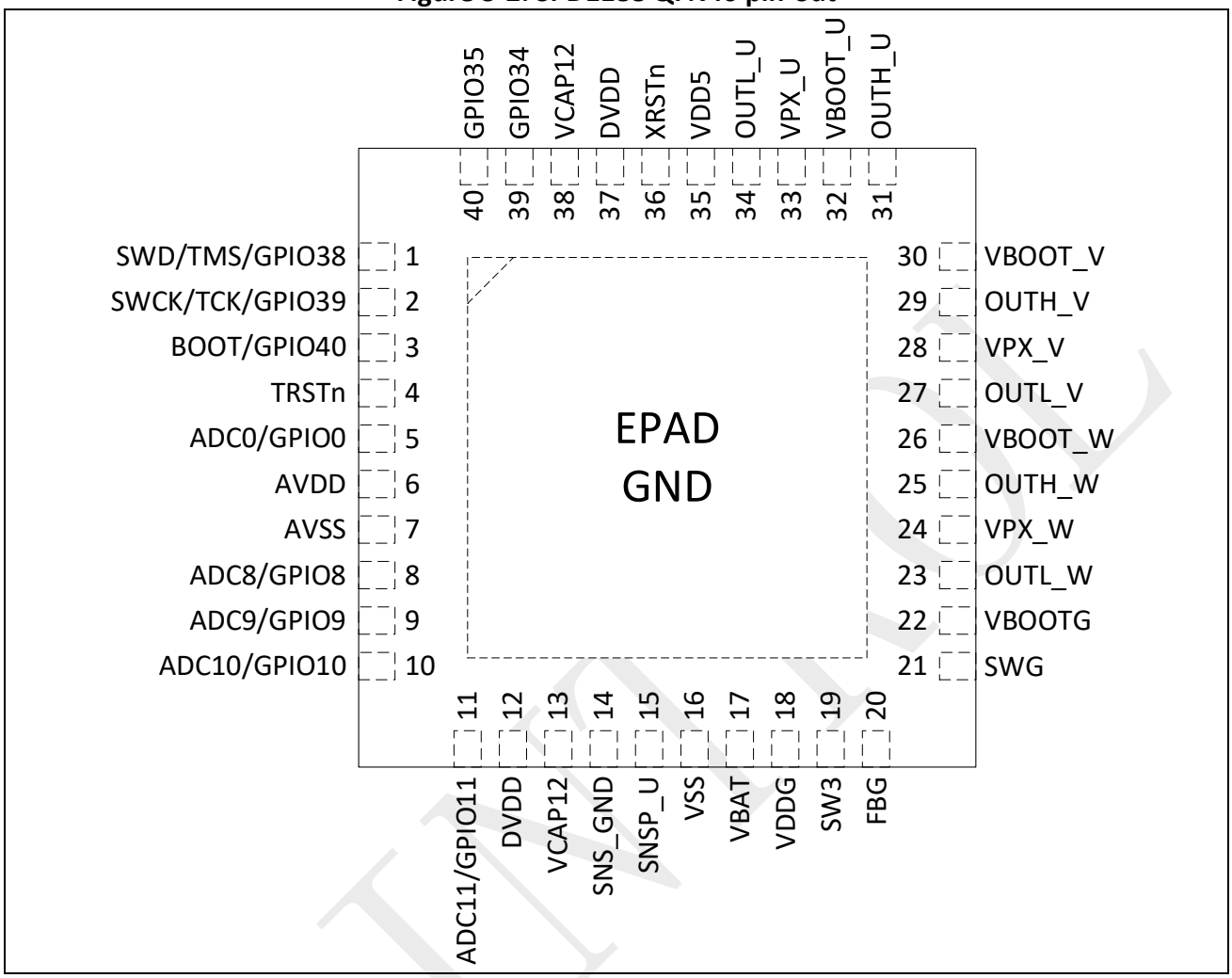
Pin	Signal	Type[1]	Description
37	VBOOT_W	O	Pre-Driver W-Phase Bootstrap Pin
38	OUTL_V	O	Pre-Driver V-Phase Low Side FET Gate Drive
39	VPX_V	O	Pre-Driver V-Phase Power FET Switching Node
40	OUTH_V	O	Pre-Driver V-Phase High Side FET Gate Drive
41	VBOOT_V	O	Pre-Driver V-Phase Bootstrap Pin
42	OUTL_U	O	Pre-Driver U-Phase Low Side FET Gate Drive
43	VPX_U	O	Pre-Driver U-Phase Power FET Switching Node
44	OUTH_U	O	Pre-Driver U-Phase High Side FET Gate Drive
45	VBOOT_U	O	Pre-Driver U-Phase Bootstrap Pin
46	VDD5	S	5V supply pin
47	XRSTn	I	Device reset pin, reset the device when low
48	DVDD	S	3.3V supply pin
49	GPIO30	I/O	General-purpose input/output 30
	SPI_SCLK	I/O	SPI clock input/output
	I2C_SCL	I/O	I^2C clock
	COMP3H	O	Comparator COMP3H result output
	PWM3A	O	PWM3 output A
	PWM0A	O	PWM0 output A
50	GPIO31	I/O	General-purpose input/output 31
	SPI_SFRM	I/O	SPI frame signal
	I2C_SDA	I/O	I^2C data
	COMP3L	O	Comparator COMP3L result output
	PWM3B	O	PWM3 output B
	PWM0B	O	PWM0 output B
51	GPIO32	I/O	General-purpose input/output 32
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	COMP4H	O	Comparator COMP4H result output
	PWM4A	O	PWM4 output A
	EPWRTZ0O	O	Trip-zone signal 0 from ePower module for monitoring
52	GPIO34	I/O	General-purpose input/output 34
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
53	GPIO35	I/O	General-purpose input/output 35
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
54	GPIO36	I/O	General-purpose input/output 36
	TDO	O	JTAG data output
	UART_RXD	I	UART receive data
	SPI_SCLK	I/O	SPI clock input/output

Pin	Signal	Type[1]	Description
	PWM5A	O	PWM5 output A
	PWM1A	O	PWM1 output A
	I2C_SDA	I/O	I^2C data
	Note: when TRSTn is HIGH, this pin always works as TDO and can't be configured as other functions.		
55	GPIO37	I/O	General-purpose input/output 37
	TDI	I	JTAG data input
	UART_TXD	O	UART transmit data
	SPI_SFRM	I/O	SPI frame signal
	PWM5B	O	PWM5 output B
	PWM1B	O	PWM1 output B
	I2C_SCL	I/O	I^2C clock
	Note: when TRSTn is HIGH, this pin always works as TDI and can't be configured as other functions.		
56	GPIO38	I/O	General-purpose input/output 38
	TMS/SWD	I/O	JTAG mode select or SWD data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	PWM2A	O	PWM2 output A
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		

[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.
[2] EPWRTZO signal is logic OR of EPWRTZ0O signal and EPWRTZ1O signal.
[3] All GPIO pins can be configured as ECAP input.
[4] All GPIO pins (except GPIO36 and GPIO37) can be configured as ECAP output.

3.2 QFN40

Figure 3-2: SPD1188 QFN40 pin-out



[1] The above figure shows the package top view.

[2] **Note: there is no need to connect the two VCAP12 pins on the PCB boards**.

[3] **Note: when TRSTn is HIGH, GPIO38 ~ GPIO39 pins work as Debug interface and can't be configured as other functions**.

Table 3-2: SPD1188 QFN40 pin definitions

Pin	Signal	Type[1]	Description
1	GPIO38	I/O	General-purpose input/output 38
	TMS/SWD	I/O	JTAG mode select or SWD data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	PWM2A	O	PWM2 output A
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		
2	GPIO39	I/O	General-purpose input/output 39
	TCK/SWCK	I	JTAG clock or SWD clock
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	PWM2B	O	PWM2 output B
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
3	BOOT(GPIO40)	I/O	Boot pin (General-purpose input/output 40)
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZ0O	O	Trip-zone signal 0 from ePower module for monitoring
	EPWRTZ1O	O	Trip-zone signal 1 from ePower module for monitoring
4	TRSTn	I	JTAG reset pin, reset the JTAG when low
5	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
6	AVDD	S	Analog power
7	AVSS	S	Analog ground
8	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
	SPI_SCLK	I/O	SPI clock input/output
	COMP3H	O	Comparator COMP3H result output
	PWMSOC	O	PWM SOC signal output for monitoring
9	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
	SPI_SFRM	I/O	SPI frame signal
10	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	COMP4H	O	Comparator COMP4H result output
11	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input

Pin	Signal	Type[1]	Description
	COMP4L	O	Comparator COMP4L result output
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZO[2]	O	Trip-zone signal from ePower module for monitoring
12	DVDD	S	Digital power
13	VCAP12	S	1.2V power
14	SNS_GND	AI	Ground sense for Motor PGA
15	SNSP_U	AI	U Phase current sense for Motor PGA
16	VSS	S	Ground
17	VBAT	S	VBAT supply pin
18	VDDG	S	V_{DDG} supply pin
19	SW3	S	LV buck switching pin
20	FBG	AI	HV buck Feedback pin
21	SWG	S	HV buck switching pin
22	VBOOTG	S	HV buck bootstrap pin
23	OUTL_W	O	Pre-Driver W-Phase Low Side FET Gate Drive
24	VPX_W	O	Pre-Driver W-Phase Power FET Switching Node
25	OUTH_W	O	Pre-Driver W-Phase High Side FET Gate Drive
26	VBOOT_W	O	Pre-Driver W-Phase Bootstrap Pin
27	OUTL_V	O	Pre-Driver V-Phase Low Side FET Gate Drive
28	VPX_V	O	Pre-Driver V-Phase Power FET Switching Node
29	OUTH_V	O	Pre-Driver V-Phase High Side FET Gate Drive
30	VBOOT_V	O	Pre-Driver V-Phase Bootstrap Pin
31	OUTH_U	O	Pre-Driver U-Phase High Side FET Gate Drive
32	VBOOT_U	O	Pre-Driver U-Phase Bootstrap Pin
33	VPX_U	O	Pre-Driver U-Phase Power FET Switching Node
34	OUTL_U	O	Pre-Driver U-Phase Low Side FET Gate Drive
35	VDD5	S	5V supply pin
36	XRSTn	I	Device reset pin, reset the device when low
37	DVDD	S	3.3V supply pin
38	VCAP12	S	1.2V power
39	GPIO34	I/O	General-purpose input/output 34
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
40	GPIO35	I/O	General-purpose input/output 35
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input

[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.
[2] EPWRTZO signal is logic OR of EPWRTZ0O signal and EPWRTZ1O signal.
[3] All GPIO pins can be configured as ECAP input.
[4] All GPIO pins can be configured as ECAP output.

3.3 PGA input channel selection

For the three on-MCU PGA's, each PGA has two 1-of-8 multiplexers (MUX) for input channel selection, one is for positive input (PGAx_P, x = 0,1,2) and the other is for negative input (PGAx_N, x = 0,1,2). The input channel selection table is shown below.

Table 3-3: PGA input channel selection

MUX Value	PGA0_P	PGA0_N	PGA1_P	PGA1_N	PGA2_P	PGA2_N
7	~~*ADC4*~~[1]	ADC3	ADC9	ADC1	~~*ADC14*~~	~~*ADC15*~~
6	ADC10	~~*ADC5*~~	ADC10	ADC11	ADC12	ADC13
5	ADC8	ADC9	ADC8	ADC10	ADC8	ADC11
4	~~*ADC6*~~	~~*ADC7*~~	ADC2	ADC3	~~*ADC4*~~	~~*ADC5*~~
3	ADC0	ADC1	ADC0	ADC2	ADC0	ADC3
2	DAC2	DAC3	ATEST	VDD12	TSEN1[2]	TSEN0[2]
1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
0	GND	GND	GND	GND	GND	GND

[1] The selections with strikeout are not available in SPD1188.

[2] TSEN0 is output 0 of T-Sensor and TSEN1 is output 1 of T-Sensor.

3.4 GPIO pin function and state after reset

Table 3-4: GPIO pin function and state after reset

Pin Name	Default Function	Default State
GPIO0	ADC0	Floating
GPIO1	ADC1	Floating
GPIO2	ADC2	Floating
GPIO3	ADC3	Floating
~~GPIO4~~	~~ADC4~~	Floating
~~GPIO5~~	~~ADC5~~	Floating
~~GPIO6~~	~~ADC6~~	Floating
~~GPIO7~~	~~ADC7~~	Floating
GPIO8	ADC8	Floating
GPIO9	ADC9	Floating
GPIO10	ADC10	Floating
GPIO11	ADC11	Floating
GPIO12	ADC12	Floating
GPIO13	ADC13	Floating
~~GPIO14~~	~~ADC14~~	Floating
~~GPIO15~~	~~ADC15~~	Floating
GPIO16	GPIO16	Floating
GPIO17	GPIO17	Floating
~~GPIO18~~	~~GPIO18~~	Floating
~~GPIO19~~	~~GPIO19~~	Floating
~~GPIO20~~	~~GPIO20~~	Floating
~~GPIO21~~	~~GPIO21~~	Floating
~~GPIO22~~	~~GPIO22~~	Floating
~~GPIO23~~	~~GPIO23~~	Floating
GPIO24	GPIO24	Floating
GPIO25	GPIO25	Floating

Pin Name	Default Function	Default State
GPIO26	GPIO26	Floating
GPIO27	GPIO27	Floating
GPIO28	GPIO28	Floating
GPIO29	GPIO29	Floating
GPIO30	GPIO30	Floating
GPIO31	GPIO31	Floating
GPIO32	GPIO32	Floating
~~GPIO33~~	~~GPIO33~~	Floating
GPIO34	GPIO34	Pull up
GPIO35	GPIO35	Pull up
GPIO36	GPIO36	Floating
GPIO37	GPIO37	Floating
GPIO38	GPIO38	Floating
GPIO39	GPIO39	Floating
GPIO40	GPIO40/BOOT	Pull up

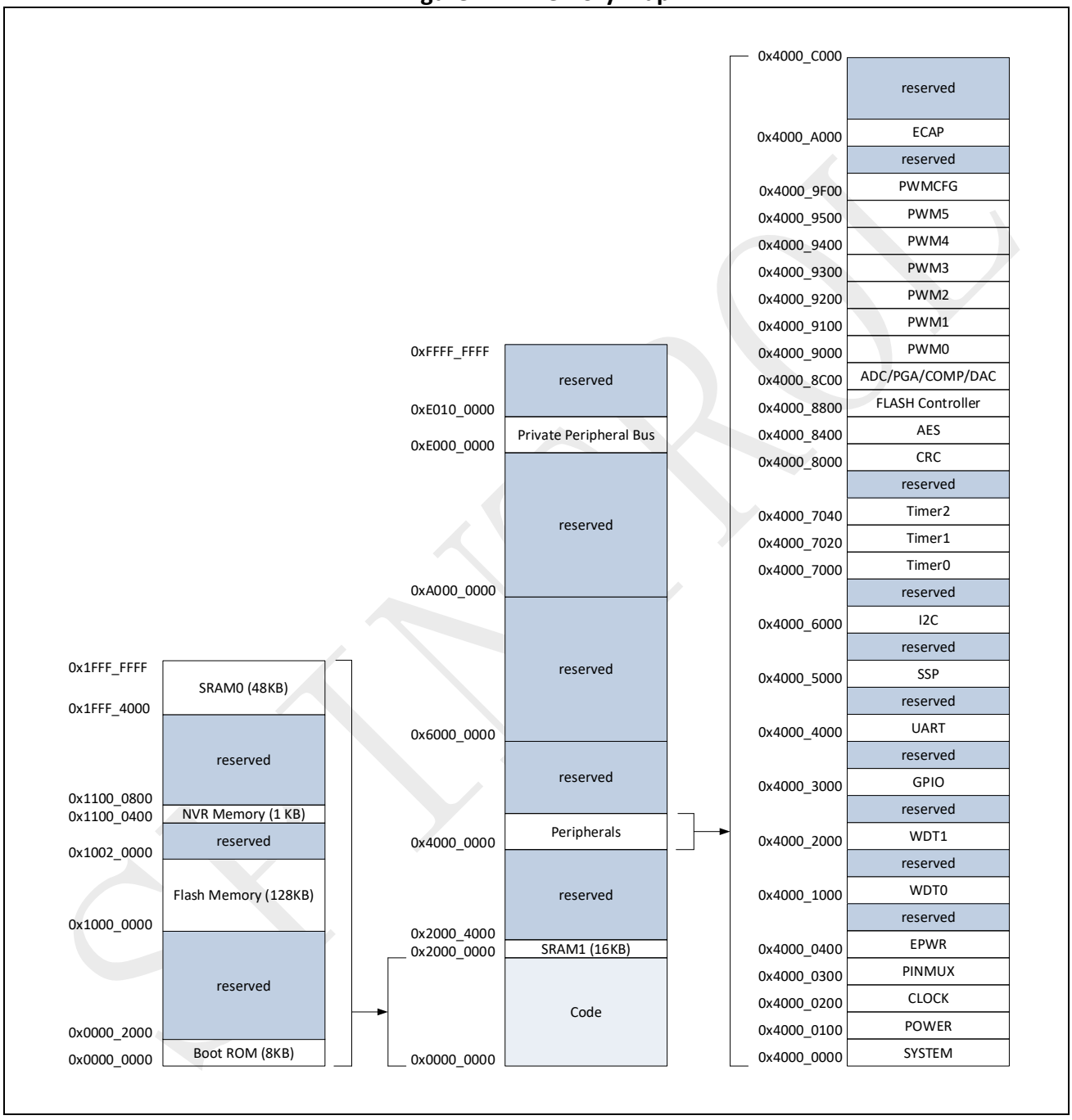
[1] In SPD1188, GPIO24~ GPIO29 are internally connected to the high voltage module, and not bonded out to the external pin.

[2] In SPD1188, the GPIOs with strikeout are not bonded out to the external pin.

4 Memory mapping

The memory map of SPD1188 is shown in Figure 4-1.

Figure 4-1: Memory map



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 5-1: Absolute maximum ratings[1][2]

Symbol	Parameter	Min	Max	Unit
V_{BAT}	Pre-Driver supply voltage, with respect to V_{SS}	9	100	V
V_{DDG}	Pre-Driver low-side gate voltage, with respect to V_{SS}	9	20	V
V_{BOOT}	Pre-Driver high-side floating power level, to V_{SS}	–	108	V
V_{DD}	Supply voltage, with respect to V_{SS}	-0.3	4.6	V
V_{DDA}	Analog voltage, with respect to V_{SSA}	-0.3	4.6	V
V_{IN}	Input voltage (V_{DD} = 3.3 V)	-0.3	4.6	V
V_O	Output voltage	-0.3	4.6	V
I_{IC}	Input clamp current	-20	+20	mA
I_{OC}	Output clamp current	-20	+20	mA
T_J	Junction temperature[3]	-40	+125	°C
T_A	Ambient temperature[3]	-40	+105	°C
T_{stg}	Storage temperature[3]	-65	+150	°C

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these is not implied.

[2] All voltage values are with respect to V_{SS}, unless otherwise noted.

[3] Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life.

5.2 Recommended operating conditions

Table 5-2: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{BAT}	Pre-Driver supply voltage	–	9	48	96	V
V_{DDG}	Pre-Driver low-side gate supply	–	9	10	18	V
V_{BOOT}	Pre-Driver High-side floating power level	–	7.3	–	104	V
V_{DD}	Supply voltage	–	2.97	3.3	3.63	V
V_{SS}	Supply ground	–	–	0	–	V
V_{DDA}	Analog supply voltage	–	2.97	3.3	3.63	V
V_{SSA}	Analog ground	–	–	0	–	V
V_{PX}	Motor driving node	–	-10	–	96	V
V_{IH}	High-level input voltage	V_{DD} = 3.3 V	2.0	–	V_{DD}+0.3	V
V_{IL}	Low-level input voltage	V_{DD} = 3.3 V	V_{SS} - 0.3	–	0.8	V
I_{OH}	High-level output source current for GPIO when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{OL}	Low-level output sink current for GPIO when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
T_J	Junction temperature	–	-40	–	+125	°C
T_A	Ambient temperature	–	-40	–	+105	°C

5.3 I/O Electrical characteristics

Table 5-3: I/O Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = I_{OH} MAX	V_{DD}-0.4	–	–	V
V_{OL}	Low-level output voltage	I_{OL} = I_{OL} MAX	–	–	0.4	V
V_{IH}	High-level input voltage	V_{DD} = 3.3 V	2.0	–	V_{DD}+0.3	V
V_{IL}	Low-level input voltage	V_{DD} = 3.3 V	V_{SS}-0.3	–	0.8	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{IL}	Low-level input current (Pin with pull-up and pull-down disabled)	V_{DD} = 3.3V, V_{IH} = 0 V	–	–	2	uA
I_{IH}	High-level input current (Pin with pull-up and pull-down disabled)	V_{DD} = 3.3V, V_{IH} = V_{DD}	–	–	2	uA
R_{PU}	Input pull-up resistor	V_{IO} = 0 V	–	41	–	kΩ
R_{PD}	Input pull-down resistor	V_{IO} = V_{DD}	–	42	–	kΩ

5.4 Power consumption summary

Typical current consumption

In operational mode, the SPD1188 is placed under the following conditions:
- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are enabled;
- All peripheral clocks are as fast as HCLK (frequency division is Zero), except SSP (Max 50 MHz) I2C (Max 50 MHz), PCLK (Max 50 MHz);
- All clock modules are enabled;
- Select PLL clock as system clock source.

In idle mode, the SPD1188 is placed under the following conditions:
- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are clocked off or disabled;
- Clock modules (PLL, RCO0 and XO) are disabled;
- Select RCO1 as system clock source.

In global deep sleep mode, the SPD1188 is placed under the following conditions:
- Both HV buck and LV buck will be disabled thus no power supply for MCU and pre-driver
- All the control blocks are disabled except reset monitoring logics used to wait for wake-up command.

In MCU-only deep sleep mode, the SPD1188 is placed under the following conditions:
- LV and HV Buck's are on;
- All I/O pins are in input mode and left unconnected;

- All peripherals (including analog module) are clocked off or disabled;
- Clock modules (PLL, RCO1 and XO) are disabled;
- 1.2V LDO is shut down to 0V.

The typical current consumption of SPD1188 measured from VBAT is shown in Table 5-4 and Table 5-5. The operational current consumption over various HCLK frequency is shown in Figure 5-1.

Table 5-4: SPD1188 typical current consumption (Run in FLASH)

Mode	Conditions (MHz)			VBAT = 24V	VBAT = 36V	VBAT = 48V	VBAT = 60V	VBAT = 72V	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}						
Operational	200[2]	50	200	9.19	7.09	5.92	4.9	4.45	mA
	175[2]	43.75	175	8.49	6.58	5.53	4.61	4.23	mA
	168[2]	42	168	8.32	6.42	5.42	4.53	4.17	mA
	150[2]	50	150	7.83	6.05	5.15	4.35	3.97	mA
	125[2]	41.67	125	7.11	5.53	4.73	4.05	3.81	mA
	100	50	100	6.4	5.05	4.32	3.76	3.32	mA
	75	37.5	75	5.66	4.52	3.9	3.45	3.19	mA
	50	50	50	4.95	3.99	3.51	3.15	2.95	mA
	32	32	32	4.33	3.56	3.15	2.92	2.73	mA
	25	25	25	4.06	3.36	2.99	2.79	2.69	mA
Idle (Pre-Driver enabled)	2.2	2.2	–	4.02	3.59	3.37	3.25	3.17	mA
Idle	2.2	2.2	–	2.99	2.62	2.44	2.32	2.25	mA
Deep Sleep	–	–	–	7.9	9.5	10.9	12.4	13.8	uA

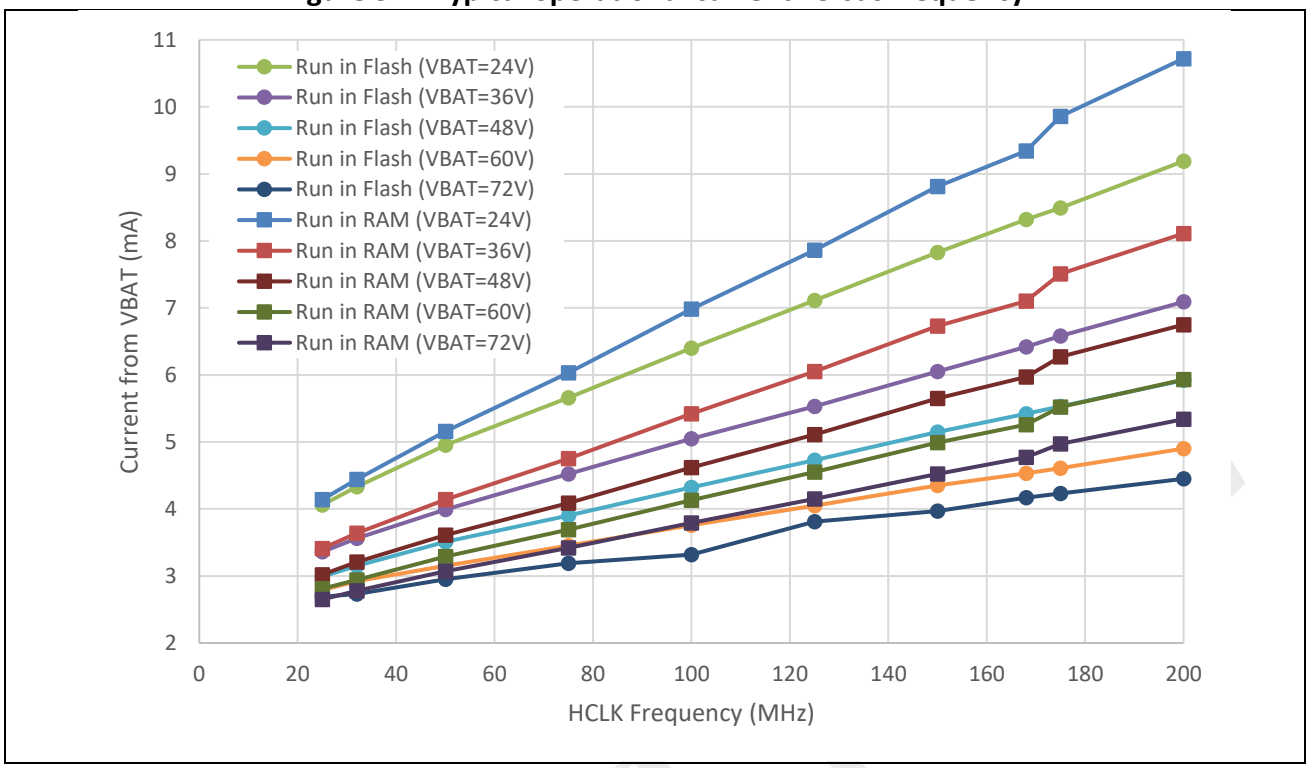
[1] Typical values are measured at T_A = 25 °C.

Table 5-5: SPD1188 typical current consumption (Run in RAM)

Mode	Conditions (MHz)			VBAT = 24V	VBAT = 36V	VBAT = 48V	VBAT = 60V	VBAT = 72V	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}						
Operational	200[2]	50	200	10.72	8.11	6.75	5.93	5.34	mA
	175[2]	43.75	175	9.86	7.51	6.27	5.52	4.97	mA
	168[2]	42	168	9.34	7.1	5.97	5.26	4.77	mA
	150[2]	50	150	8.81	6.73	5.65	4.99	4.52	mA
	125[2]	41.67	125	7.86	6.05	5.11	4.55	4.15	mA
	100	50	100	6.98	5.42	4.62	4.13	3.79	mA
	75	37.5	75	6.03	4.75	4.09	3.69	3.42	mA
	50	50	50	5.16	4.14	3.61	3.29	3.07	mA
	32	32	32	4.44	3.64	3.21	2.94	2.78	mA
	25	25	25	4.14	3.41	3.02	2.81	2.65	mA
Idle (Pre-Driver enabled)	2.2	2.2	–	3.99	3.52	3.3	3.18	3.11	mA
Idle	2.2	2.2	–	2.99	2.61	2.41	2.29	2.21	mA

[1] Typical values are measured at T_A = 25 °C.

Figure 5-1: Typical operational current versus frequency



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 5-6. The MCU is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals(including analog module, RCO0 and XO) are disabled unless otherwise mentioned;
- The given value is calculated by measuring the current consumption
  - With all peripherals clocked disabled
  - With only one peripheral enabled

Table 5-6: Peripheral current consumption

Peripherals[1]		Conditions	Typ[2]	Unit
BOD		Select RCO0 as system clock source; All other peripherals are in default settings; Close PLL, XO, RCO1 and RCO0 after disabling or enabling BOD module	0.1	mA
ADC	Analog[3]	Select PLL clock as system clock source; All peripheral clocks are as fast as HCLK; f_{HCLK} = 128 MHz, f_{PCLK} = 32 MHz, f_{PLL} = 128 MHz	16.52	mA
	Digital		0.31	mA
T-Sensor			0.16	mA
PGA[4]			4.10	mA
DAC			0.18	mA
Comparator			0.08	mA
UART		UART clock 200MHz, 256000 bps	0.416	mA
I2C		I2C clock 50MHz, 2Mbps	0.316	mA
SSP		SSP clock 50MHz, 50Mbps	0.361	mA
PWM		PWM clock 200MHz	1.471	mA
ECAP		ECAP clock 200MHz	0.329	mA
WDT		WDT clock 200MHz	0.245	mA
TMR		TMR clock 200MHz	0.385	mA
FLASH		HCLK clock 200MHz	0.772	mA
XO		HCLK is from 200MHz PLL, which takes RCO0 as input	0.616	mA
RCO		HCLK is from 200MHz PLL, which takes XO as input	0.313	mA
PLL		XO as HCLK source, f_{PLL} = 32 MHz	1.153	mA

[1] For peripherals with multiple instances, the current quoted is for single modules. For example, the 4.10 mA value quoted for PGA is for one PGA module. So the total 3 PGA module current is 12.30mA.

[2] Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.

[3] ADC analog current contain ADC analog module, bandgap and ADC reference buffer.

[4] The Bandgap must be enabled when enabling ADC (Analog Part), T-sensor, PGA, DAC and comparator.

5.5 Internal 1.2V regulator characteristics

Table 5-7: Internal 1.2V regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Power supply	–	2.97	3.3	3.63	V
VCAP12	Output voltage	Load current = 50mA	1.18	1.20	1.22	V
ΔVCAP12	Load regulation	VCAP12(50mA load) - VCAP12(200mA load)	–	–	30	mV

Figure 5-2: Internal 1.2V regulator load regulation (T_A = 25 °C)

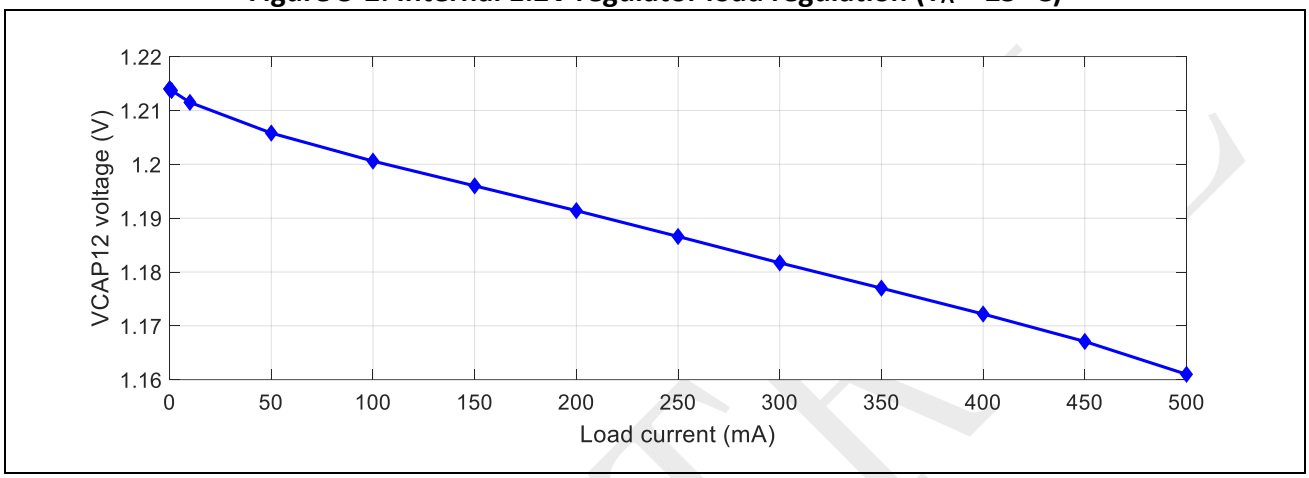
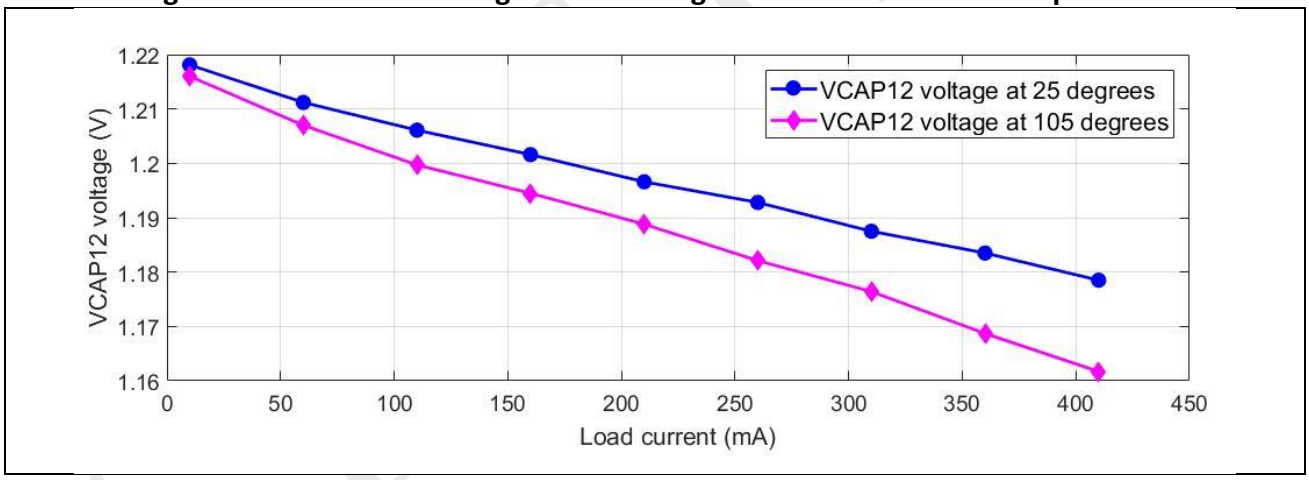


Figure 5-3: Internal 1.2V regulator load regulation with different temperature



5.6 BOD characteristics

Table 5-8: BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	–	2.97	3.3	3.63	V
V_{DD33H_Asset}	VDD33 too high assert threshold	–	–	3.42	–	V
$V_{DD33H\_Deasset}$	VDD33 too high de-assert threshold	–	–	3.31	–	V
V_{DD33L_Asset}	VDD33 too low assert threshold	–	–	2.58	–	V
$V_{DD33L\_Deasset}$	VDD33 too low de-assert threshold	–	–	2.65	–	V
V_{DD12H_Asset}	VDD12 too high assert threshold	–	–	1.33	–	V
$V_{DD12H\_Deasset}$	VDD12 too high de-assert threshold	–	–	1.31	–	V
V_{DD12L_Asset}	VDD12 too low assert threshold[1]	–	–	0.94	–	V
$V_{DD12L\_Deasset}$	VDD12 too low de-assert threshold[1]	–	–	0.97	–	V

[1] The characteristics of VDD12 too low 0 and VDD12 too low 1 are the same.

5.7 RCO characteristics

Table 5-9: RCO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	–	2.97	3.3	3.63	V
f_{RCO}	RCO frequency at room temperature	T_J = 25 °C	–	32	–	MHz
ACC_{RCO}	RCO frequency accuracy (RCO frequency variation versus temperature)	T_J = -40~125 °C	-1	–	1	%

5.8 PLL characteristics

Table 5-10: PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	–	2.97	3.3	3.63	V
f_{VCO}	VCO frequency	–	400	500	600	MHz
f_{pfd}	Phase-Frequency Detector (PFD) input frequency	–	4	–	8	MHz
t_{LOCK}	Locking time	–	–	–	15	us

5.9 XO characteristics

Table 5-11: XO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	–	2.97	3.3	3.63	V
F_{XO}	XO frequency	–	1	–	66	MHz

The negative resistance of the on-chip crystal oscillator at different temperature is shown in Figure 5-4 ~ Figure 5-7. The loading capacitor CL_eff is defined as equivalent capacitance seen by the on-chip crystal.

Figure 5-4: The negative resistance of the on-chip crystal oscillator at 50 °C

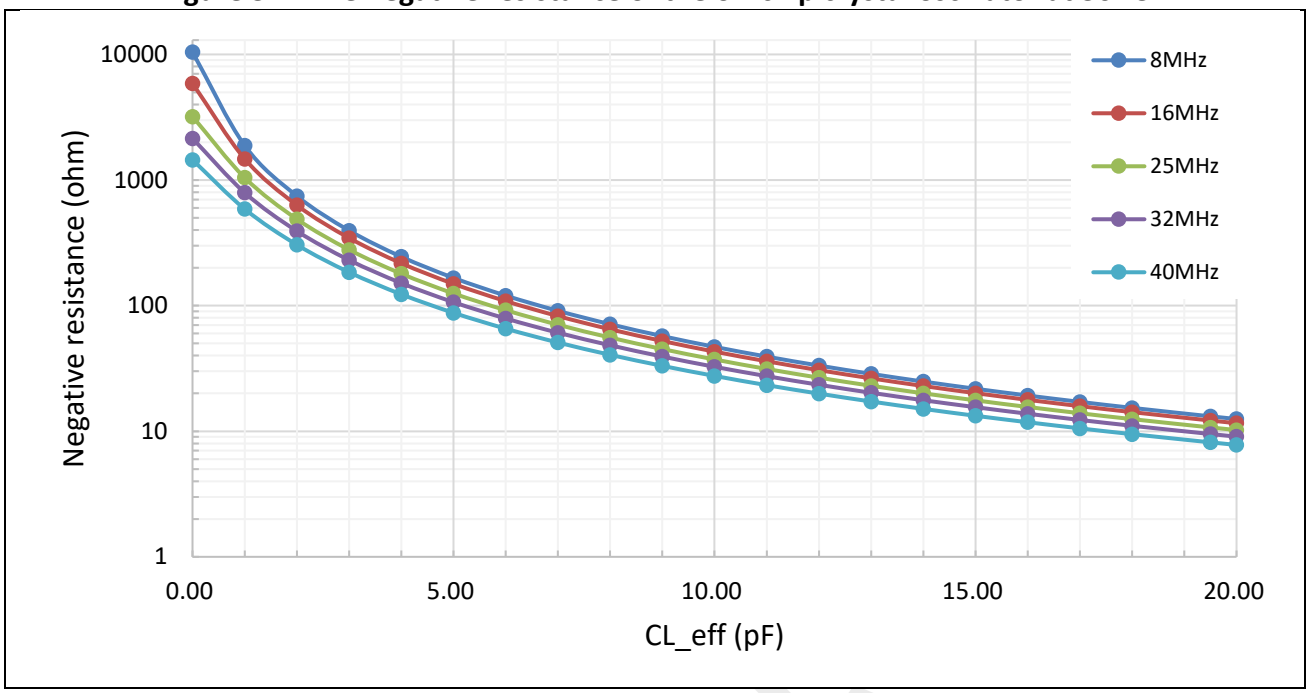


Figure 5-5: The negative resistance of the on-chip crystal oscillator at 85 °C

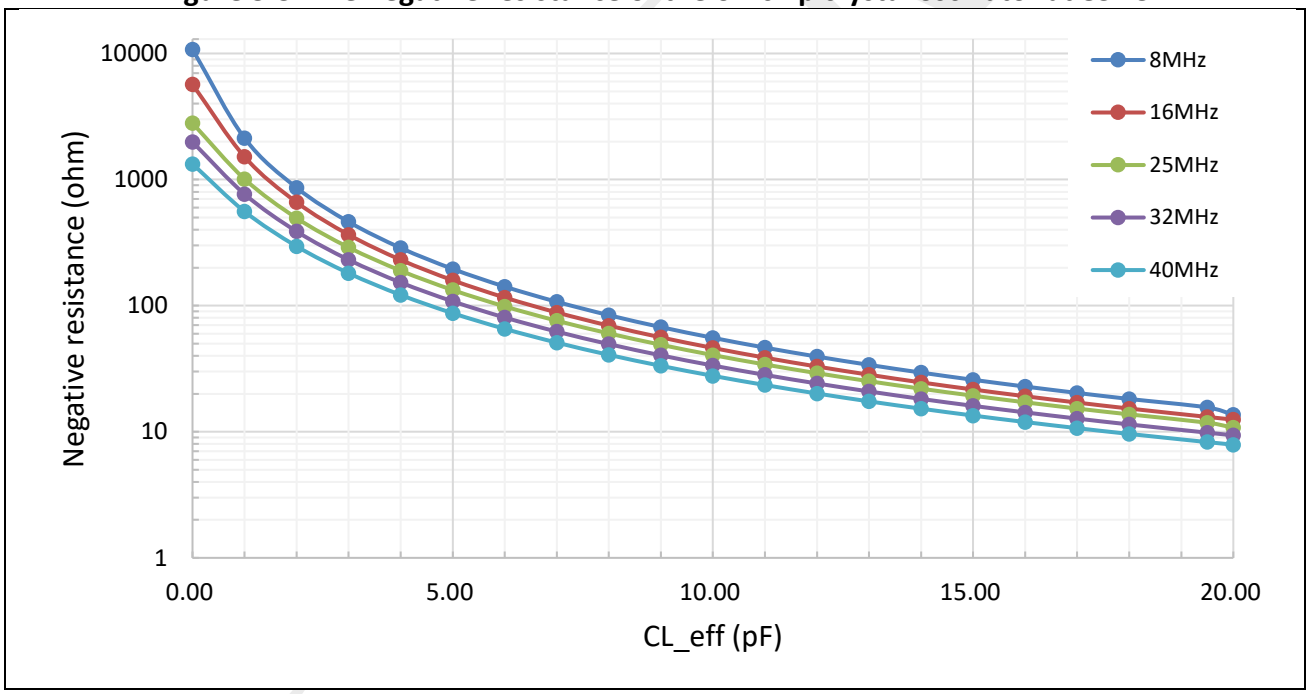


Figure 5-6: The negative resistance of the on-chip crystal oscillator at 100 °C

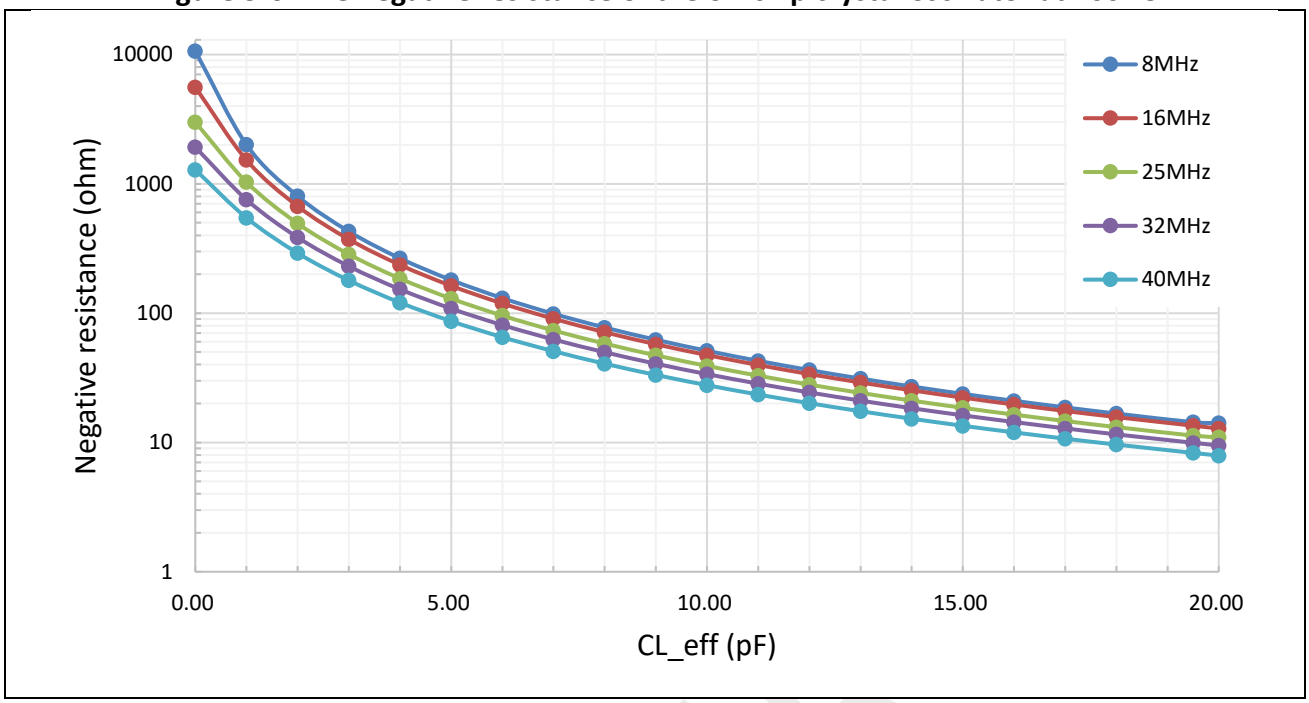
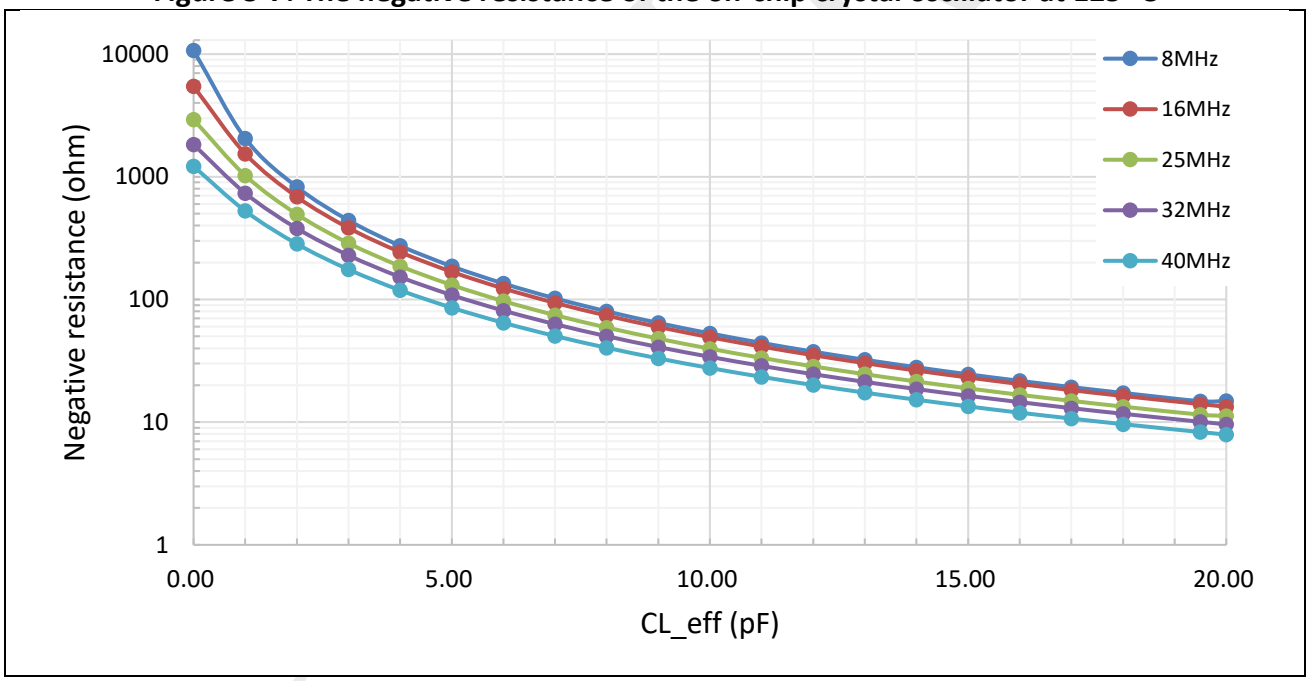


Figure 5-7: The negative resistance of the on-chip crystal oscillator at 125 °C



5.10 14-bit ADC characteristics

Table 5-12: ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	–	2.97	3.3	3.63	V
N_R	Resolution	No missing code. Monotonic	14	–	–	bit
F_S	Conversion speed[1]	–	–	–	4	MSPS
V_{AIN}	Input voltage range	–	0	–	V_{DDA}	V
V_{REF}	Reference voltage	–	1.194	1.2	1.206	V
I_{PAD}	Operational current	V_{DDA} = 3.3V	–	17.1	21	mA
INL	Integral linearity error	–	-3.0	–	3.0	LSB
DNL	Differential linearity	–	-1.0	–	1.0	LSB
E_{OFF}	Offset error[2]	With calibration	-2	–	2	LSB
E_{GAIN}	Gain error[2]	With calibration	-4	–	4	LSB
E_{OFF2}	Channel to channel offset	–	-3	–	3	LSB
E_{GAIN2}	Channel to channel gain error	–	-5	–	5	LSB
T_{COEF}	ADC temperature coefficient with internal reference	–	–	26	–	ppm/°C
t_{PWRUP}	Power-up time	–	–	–	200	us
$ENOB_{DC}$	DC Noise Floor	–	–	12.0	–	bits
SNR	Signal-to-noise ratio	Fin = 100kHz Amp = 0.94F_S N = 8192	–	75.5	–	dB
THD	Total harmonic distortion		–	-85.0	–	dB
ENOB	Effective number of bits		–	12.2	–	bits
SFDR	Spurious free dynamic range		–	86.0	–	dB
T_{SLOPE}	Degrees C of temperature movement per measure ADC LSB change of the temperature sensor	–	–	1.904[3]	–	°C/LSB
T_{OFFSET}	ADC output at 25 °C of the temperature sensor	–	–	162.138	–	LSB

[1] Sampling time = 110ns, conversion time = 140ns.
[2] Offset and gain can be calibrated automatically by HW.
[3] Can be reduced to 0.24 °C/LSB by PGA.

5.11 PGA characteristics

Table 5-13: PGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	–	2.97	3.3	3.63	V
V_{AIN}	Input voltage range	–	0	–	V_{DDA}	V
V_{OUT}	Output voltage range	–	0.3	–	V_{DDA}-0.3	V
R_{IN}	Input impedance	–	–	10	–	MΩ
G	Gain	Single-ended mode	1, 2, 4, 8, 12, 16, 24, 32			–
		Differential mode	2, 4, 8, 16, 24, 32, 48, 64			–
E_{GAIN}	Gain error	Differential Gain = 2	-0.5	–	0.5	%
		Differential Gain = 64	-3	–	3	%
V_{OS}	Offset	–	-5	–	5	mV
T_{OFFSET}	Offset temperature drift	–	–	5	–	uV/°C
SR	Slew rate	Single mode and Loading is ADC sampling capacitor	–	20	–	V/us
		Differential mode and Loading is ADC sampling capacitor	–	40	–	V/us
GBW	Gain band width	Single gain = 1	–	40	–	MHz
		Single gain = 8	–	6.8	–	MHz
		Single gain = 32	–	1.7	–	MHz
		Differential gain = 2	–	20	–	MHz
		Differential gain = 16	–	3.4	–	MHz
		Differential gain = 64	–	0.8	–	MHz
t_{SETTLE}	Settle time	Differential gain = 2	–	170[1]	220	ns
		Differential gain = 16	–	400	600	ns
		Differential gain = 64	–	1600	2200	ns
SNR	Signal-to-noise ratio	Differential gain = 2 Fin = 10kHz Amp = 0.94F_S N = 8192	–	74.0	–	dB
THD	Total harmonic distortion		–	-78.0	–	dB
ENOB	Effective number of bits		–	11.6	–	bit
SFDR	Spurious free dynamic range		–	82.0	–	dB
SNR	Signal-to-noise ratio	Differential gain = 64 Fin = 10kHz Amp = 0.94F_S N = 8192	–	58.0	–	dB
THD	Total harmonic distortion		–	-80.0	–	dB
ENOB	Effective number of bits		–	9.4	–	bit
SFDR	Spurious free dynamic range		–	63.0	–	dB
I	Current consumption	Only one PGA	–	4.16	5.20	mA

[1] Settle time is measured by step input, and differential output change from -2.7V to 2.7V (VDDA=3.3V), the time for output to be settled with 1LSB (446uV), guarantee by design.

5.12 Motor PGA characteristics

Table 5-14: Motor PGA characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Power supply	–	3	3.3	3.6	V
Temp	Temperature range	–	-40	50	150	°C
V_{AIN}	Input voltage range	–	-2	0	2	V
V_{OUT}	Output voltage range	–	0.3	–	V_{DDA}-0.3	V
R_{IN}	Input impedance	–	–	4	–	kΩ
G	Gain	–	1,2,4,8,12,16,32,64			–
G_{ERR}	Gain error	Gain = 64	-1.00	–	1.00	%
V_{OS}	Offset	Gain = 64	–	–	–	mV
t_{SETTLE}	Settling time	Gain = 64	–	814	4087	ns
		Gain = 2	–	230	337	ns
ENOB	Effective number of bits	Gain = 64	9.9	10.2	10.5	bit
THD	Total harmonic distortion	Gain = 64, 100kHz	-81	–	-55	dB
IVDD	Current consumption	One PGA (V_{DDA} = 3.3V)	–	2.6	–	mA
CMR	Common mode rejection	With mismatch and V_{OUT} = 2.7V	–	–	-47	dB

5.13 Analog comparator characteristics

Table 5-15: Comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	–	2.97	3.3	3.63	V
V_{OFFSET}	Offset voltage (Hysteresis voltage=0)	Common mode input voltage = 1.65V	-10	–	10	mV
V_{HYST}	Hysteresis voltage(12mV)	–	–	13	–	mV
	Hysteresis voltage(24mV)	–	–	26	–	mV
	Hysteresis voltage(36mV)	–	–	42	–	mV
t_D	Delay time – comparator response time to PWM shunt down (Asynchronous)	–	–	50	–	ns

5.14 Internal 10-bit DAC characteristics

Table 5-16: DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	–	2.97	3.3	3.63	V
N	Resolution	Monotonic	10	–	–	bit
V_{FS}	Full scale value	–	0	–	V_{DDA}	V
DNL	Differential linearity	–	-0.5	–	0.5	LSB
INL	Integral linearity	–	-1	–	1	LSB
E_{OFF}	Offset error	–	–	5	–	mV
t_{SETTLE}	DAC settling time	Design guarantee	–	–	1	us

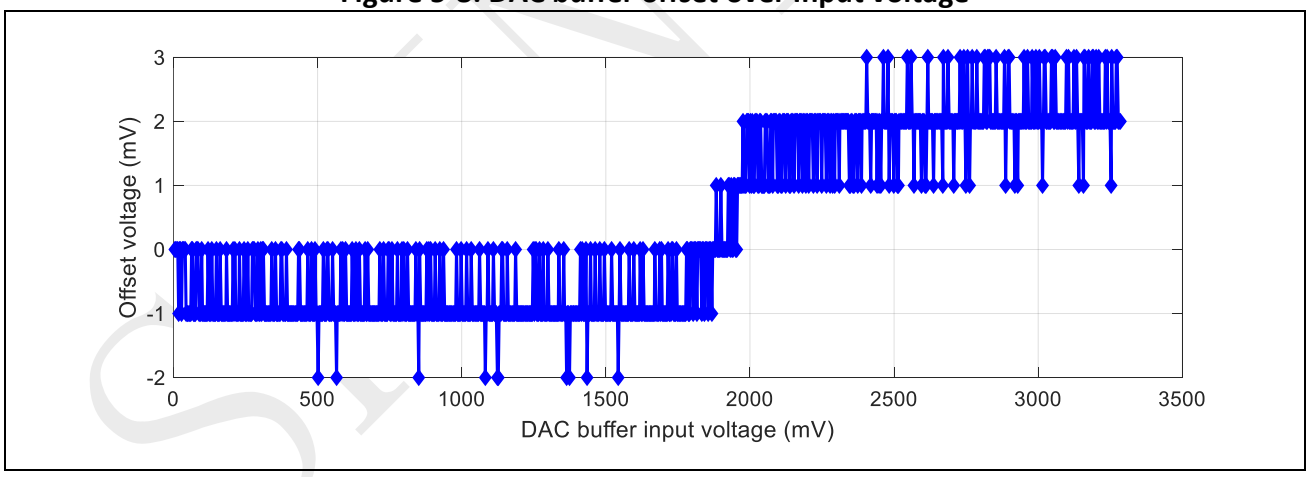
[1] The DAC is used to generate a static voltage as a threshold for the comparator and does not guarantee the performance of the waveform produced by dynamically changing the code value.

5.15 DAC buffer characteristics

Table 5-17: DAC buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	–	2.97	3.3	3.63	V
V_{OUT}	Output voltage range	–	0.3	–	V_{DDA}-0.3	V
t_{SETTLE}	Settling time	Design guarantee	–	1	–	us
E_{OFF}	Offset error	–	–	3	–	mV
CL	Capacitor load	–	–	–	50	pF
RL	Resistor load	–	1	–	–	MΩ

Figure 5-8: DAC buffer offset over Input voltage



5.16 Flash memory characteristics

The characteristics are given at T_J = -40 to 125 °C unless otherwise specified.

Table 5-18: Flash memory characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{RD}	Read access time	–	40	–	ns
t_{PROG}	Word (32-bit) program time	–	8	10	us
t_{SE}	Sector erase time	–	0.8	4	ms
t_{CE}	Chip erase time	–	8	10	ms
N_{END}	Endurance (erase/program cycle)	T_J = 85 °C	100000	–	cycles
t_{RET}	Data retention duration	T_J = 85 °C	10	–	years

5.17 Electrical sensitivity characteristics

Table 5-19: ESD absolute maximum ratings

Symbol	Parameter	Conditions		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	Ambient temperature T_A = 25 °C		2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)	Ambient temperature T_A = 25 °C	–	500	V
			Corner Pin	750	V

Table 5-20: Electrical sensitivities

Symbol	Parameter	Conditions	Max	Unit
LU	Static latch-up	Ambient temperature T_A = 85 °C V_{DD} = 3.63V, VCAP12 = 1.32V	200	mA

5.18 Moisture sensitivity characteristics

Table 5-21: Moisture sensitivity characteristic

Symbol	Parameter	Conditions	Level	Unit
MSL	Moisture sensitivity level	–	Level 3	–

5.19 Thermal resistance characteristics

Table 5-22: Thermal resistance characteristics (QFN56 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	–	9.17	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	54.93	°C/W
		4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	32.34	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

Table 5-23: Thermal resistance characteristics (QFN40 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	–	11.07	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	62.25	°C/W
		4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	37.19	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

5.20 SPI characteristics

Table 5-24: SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	–	–	–	50	MHz
$t_{SCLK(H)}$	SCLK clock high time	–	10	–	–	ns
$t_{SCLK(L)}$	SCLK clock low time	–	10	–	–	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	–	–	–	9.5	ns
$t_{H(MO)}$	Data output hold time	–	3.9	–	–	ns
$t_{SU(MI)}$	Data input setup time	–	6	–	–	ns
$t_{H(MI)}$	Data input hold time	–	2	–	–	ns
SPI slave mode						
$t_{SU(SFRM)}$	SFRM enable setup time	–	5.6	–	–	ns
$t_{H(SFRM)}$	SFRM enable hold time	–	1.5	–	–	ns
$t_{A(SO)}$	Data output access time	–	4	–	10	ns
$t_{DIS(SO)}$	Data output disable time	–	4	–	10	ns
$t_{V(SO)}$	Data output valid time	–	–	–	9.5	ns
$t_{H(SO)}$	Data output hold time	–	3.9	–	–	ns
$t_{SU(SI)}$	Data input setup time	–	6	–	–	ns
$t_{H(SI)}$	Data input hold time	–	2	–	–	ns

5.21 Pre-Driver characteristics

Table 5-25: Pre-Driver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	Input supply voltage	–	9	–	96	V
D_{MAX}	Maximum supported duty cycle	Charge pump will replenish bootstrap capacitor when high side is turned on	–	100	–	%
t_{DL}	Low-side propagation delay	1nF Capacitor as load	–	25	40	ns
t_{DH}	High-side propagation delay	1nF Capacitor as load	–	25	40	ns
Δt	High/Low side delay mismatch	–	–	–	8	ns
t_r	Rise time	1nF Capacitor as load	–	13	–	ns
t_f	Fall time	1nF Capacitor as load	–	11	–	ns
VPX_{MIN}	High side return ground Minimum	Min voltage where high side signal still propagates	-10	–	–	V
I_{Source_Max}	Pre-Driver Max sourcing capability	–	–	2	–	A
I_{Sink_Max}	Pre-Driver Max sinking capability	–	–	2	–	A

5.22 HV Buck DC/DC regulator characteristics

Table 5-26: HV Buck DC/DC regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT_Max}	Max operating voltage	–	–	–	96	V
$V_{BAT\_UV\_Trigger}$	Under voltage trigger threshold	–	–	7.65	–	V
$V_{BAT\_UV\_Release}$	Under voltage release threshold	–	–	8.15	–	V
VDDG	Pre-Driver swing voltage	VDDG = 10V	9.5	10	10.5	V
R_{ON_HS}	High side Ron	300mA	–	1.68	–	Ω
R_{ON_LS}	Low side Ron	300mA	–	0.8	–	Ω
I_{Limit}	Valley current limit	–	–	320	–	mA
η	Power efficiency	V_{BAT} = 48V 200mA, 600KHz	–	87	–	%

5.23 LV Buck DC/DC regulator characteristics

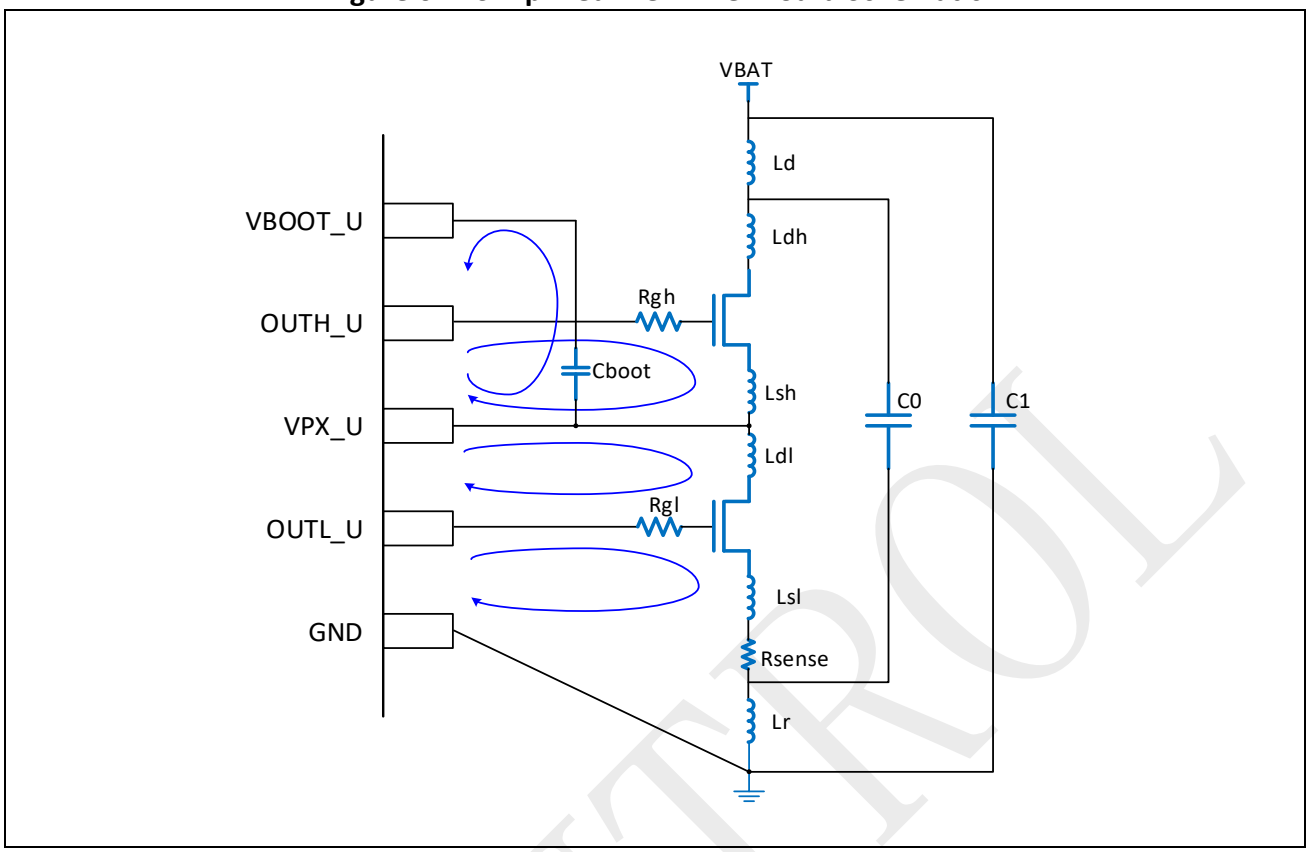
Table 5-27: LV Buck DC/DC regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDG_Max}	Max operating voltage	–	–	–	20	V
$V_{VDDG\_UV\_Trigger}$	Under voltage trigger threshold	–	–	6.2	–	V
$V_{VDDG\_UV\_Release}$	Under voltage release threshold	–	–	6.5	–	V
DVDD	3.3V output	–	3.14	3.3	3.47	V
R_{ON_HS}	High side Ron	300mA	–	1.1	–	Ω
R_{ON_LS}	Low side Ron	300mA	–	0.4	–	Ω
I_{Limit}	Valley current limit	–	–	600	–	mA
η	Power efficiency	V_{BAT} = 12V 200mA, 1.2MHz	–	90	–	%

6 PCB layout guidance

- Connect low-ESR bypass capacitors from V_{BAT}, V_{DDG}, DVDD, V_{DD5}, VCAP12, VCP to ground, placing capacitors as close as possible to their respective pins, with the other end of each capacitor having a strong connection to board ground.
- Enough through holes should be put under the chip EPAD for a good connection to the copper ground plate. This is essential for thermal dissipation.
- Put ceramic 10nF the bootstrap cap between VBOOTG and SWG pin as close to the chip as possible.
- For both HV buck and LV buck, output capacitor should be put close to the inductor, and the ground connection should be tied to IC ground VSS through short trace or copper plate.
- Co-locate power FET pairs with drain of low-side adjacent to source of high-side to minimize both Lsh and Ldl, and pairs placed close to each other to reduce routing distance and minimize Lr and Ld.
- Use thick, direct tracks between FET's with no loops or deviation.
- Minimize the areas of major current paths shown by arrows in the diagram of Figure 6-1 to avoid any loops.
- In case of standing power FET's, reduce the effect of lead inductances by lowering package height above PCB.
- Connect the other end of C0 (shown in Figure 6-1) as close as possible to the drain of high-side FET, in order to provide the lowest-parasitic return path for current.
- Place IC closer to power switches; route gate driver control signals OUTH and OUTL, and high- and low-side return grounds VPX and GND with straight as-short-as-possible traces.
- Connect bootstrap capacitor as close as possible to VPX and VBOOT pins.
- Use power FET's with fast body diode turn-on times and as small as possible diode reverse charges.
- DVDD is the feedback of buck DCDC, in order to keep the stable operation of control loop, it is recommended to keep DVDD trace away from high voltage switching trace and noisy source, such as inductor, etc.
- Keep the switching trace as short and wide as practical in order to minimize radiated emissions.
- The GND trace between the DVDD capacitor and the GND pin should be as wide as possible so that trace impedance is minimized.

Figure 6-1: Simplified Pre-Driver Board Schematic



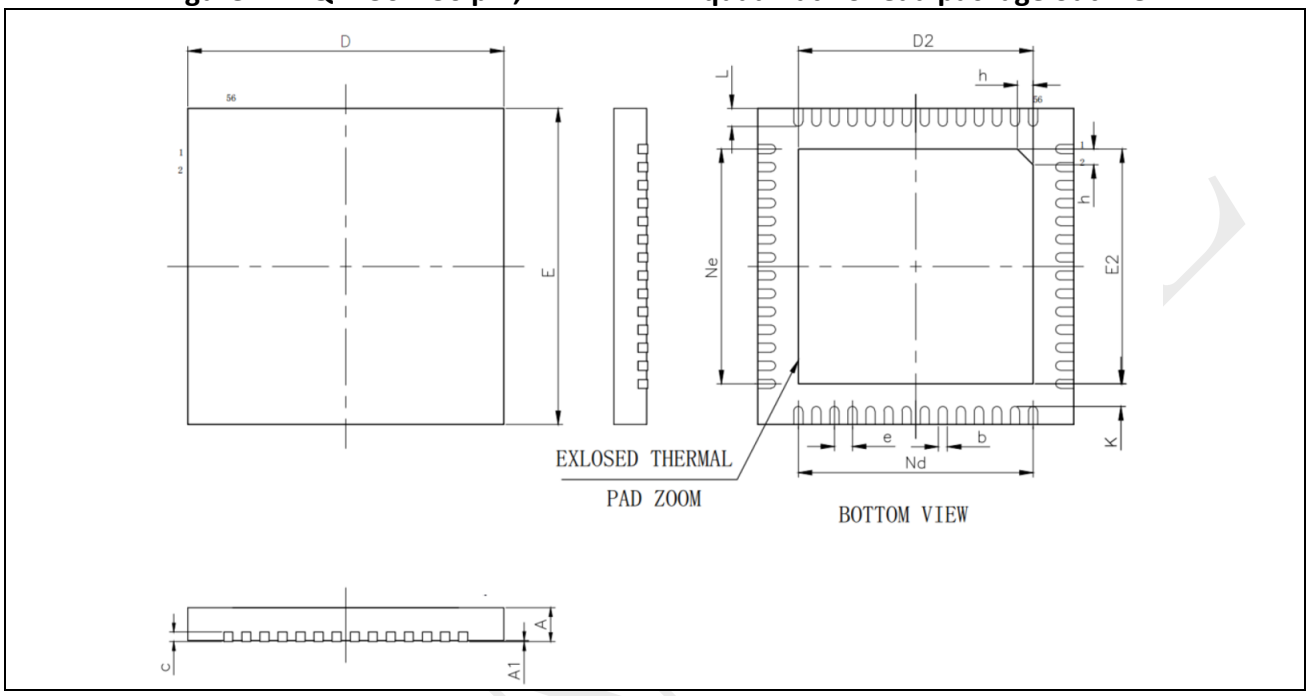
[1] This figure only shows the Pre-Driver U-phase circuit diagram. And the Pre-Driver V-phase and W-phase circuit diagrams are the same.

7 Package information

The package type of SPD1188 is 56-pin or 40-pin QFN. The detail information is as follows:

7.1 QFN56

Figure 7-1: QFN56 – 56 pin, 7mm x 7mm quad flat no-lead package outline

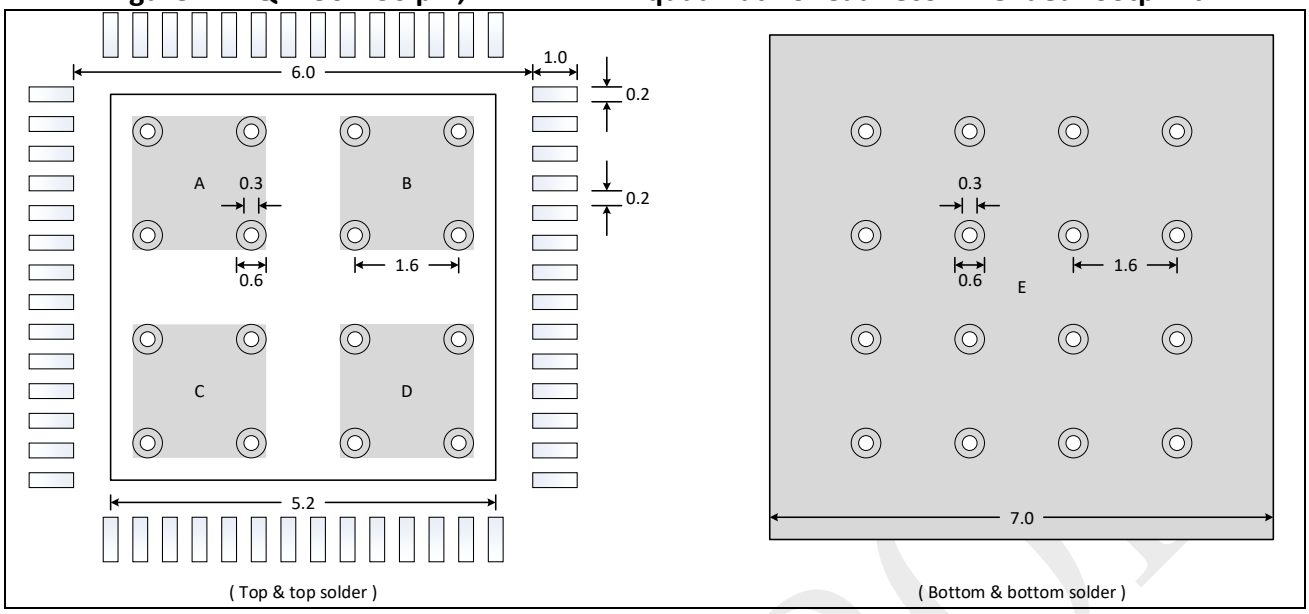


[1] Drawing is not to scale.

Table 7-1: QFN56 – 56 pin, 7mm x 7mm quad flat no-lead package mechanical data

Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.8
A1	–	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.10	5.20	5.30
e	0.40		
Ne	5.20		
Nd	5.20		
E	6.90	7.00	7.10
E2	5.10	5.20	5.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 7-2: QFN56 – 56 pin, 7mm x 7mm quad flat no-lead recommended footprint



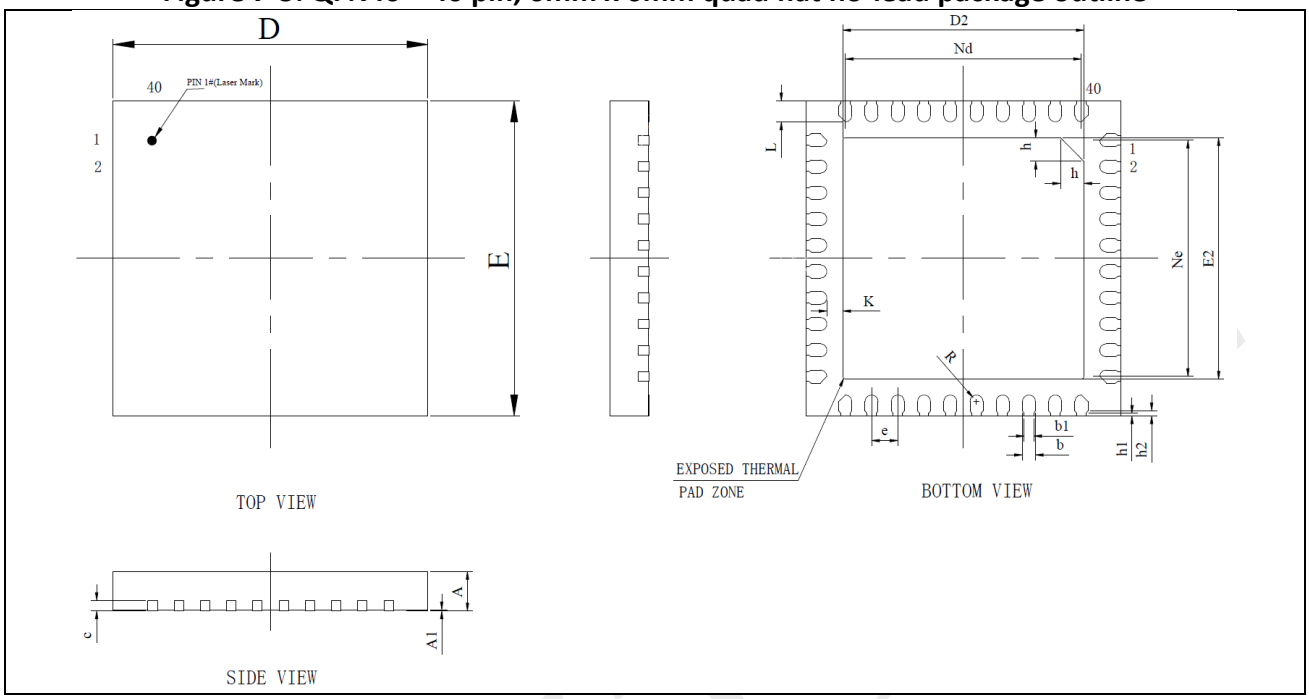
[1] Dimensions are expressed in millimeters.

[2] The A, B, C, D areas on the top layer should brush solder paste, and E area on bottom layer can either brush solder paste or not.

7.2 QFN40

7.2.1 Package Specification

Figure 7-3: QFN40 – 40 pin, 6mm x 6mm quad flat no-lead package outline



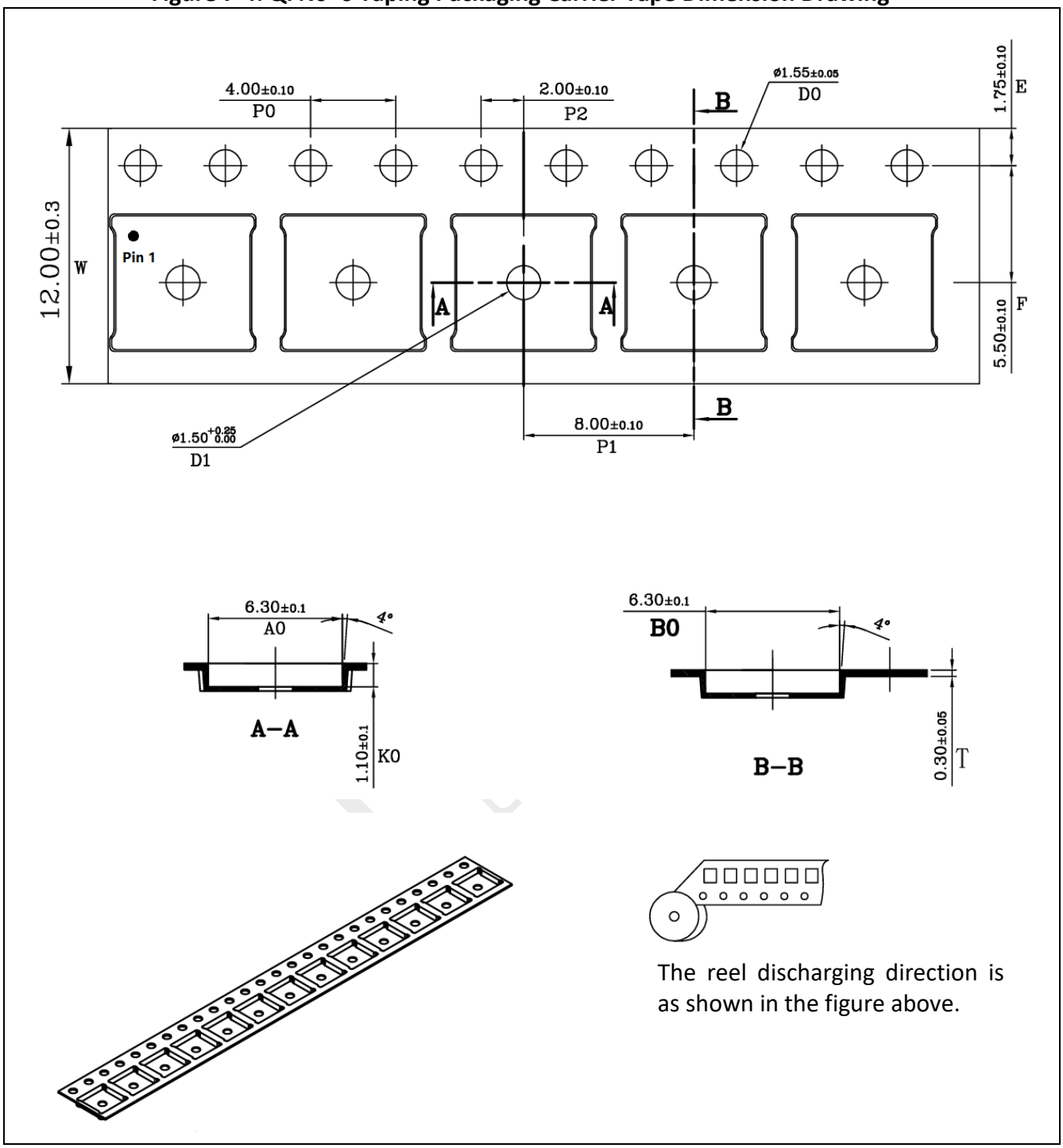
[1] Drawing is not to scale.

Table 7-2: QFN40 – 40 pin, 6mm x 6mm quad flat no-lead package mechanical data

Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.3
b1		0.18 REF	
c		0.203 REF	
D	5.90	6.00	6.10
D2	4.50	4.60	4.70
e		0.50 BSC	
Nd		4.50 BSC	
E	5.90	6.00	6.10
E2	4.50	4.60	4.70
Ne		4.50 BSC	
L	0.35	0.40	0.45
R	0.08	0.13	0.18
K		0.30 REF	
h	0.40	0.45	0.50
h1		0.05 REF	
h2		0.10 REF	

7.2.2 Packing Specification

Figure 7-4: QFN6*6 Taping Packaging Carrier Tape Dimension Drawing



[1] Drawing is not to scale.

[2] Pin 1 is located at the top left corner.

Figure 7-5: QFN6*6 Taping Packaging Reel

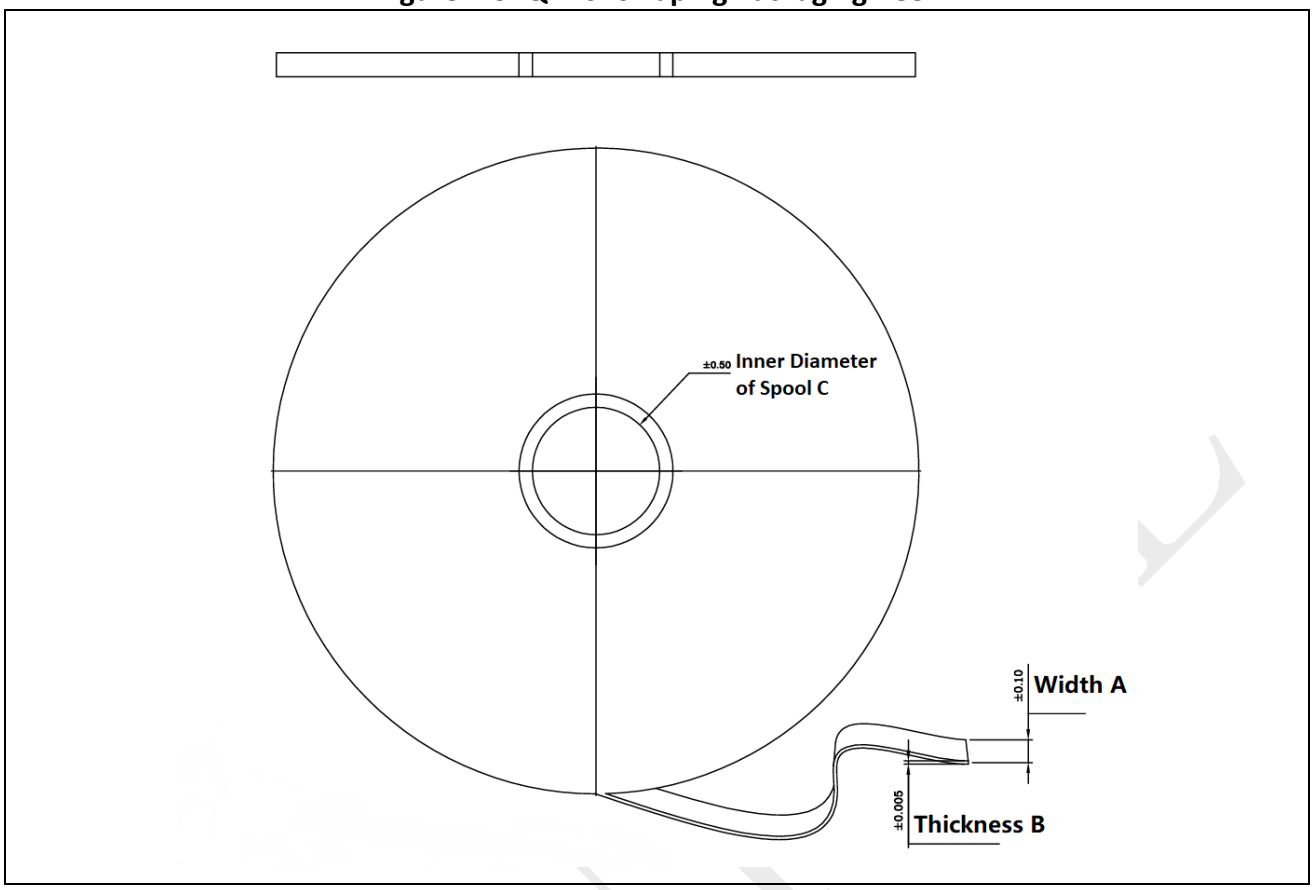


Table 7-3: Reel Dimension

Spec.	A	B	C
Dim.	13.30±0.10	0.051±0.005	76.5±0.5

8 Ordering information

Table 8-1: Ordering information

Ordering Number	Flash	SRAM	Max CPU Frequency	Package	Temperature Range	SPQ[1]	Packing
SPD1188API56	128KB	64KB	200MHz	QFN56	Industrial -40 °C to +125 °C	2600	Tray
SPD1188ZAPI56	64KB	32KB	200MHz	QFN56	Industrial -40 °C to +125 °C	2600	Tray
SPD1188YAPI56	32KB	16KB	200MHz	QFN56	Industrial -40 °C to +125 °C	2600	Tray
SPD1188XAPI56	128KB	64KB	100MHz	QFN56	Industrial -40 °C to +125 °C	2600	Tray
SPD1188WAPI56	64KB	32KB	100MHz	QFN56	Industrial -40 °C to +125 °C	2600	Tray
SPD1188VAPI56	32KB	16KB	100MHz	QFN56	Industrial -40 °C to +125 °C	2600	Tray
SPD1188API40	128KB	64KB	200MHz	QFN40	Industrial -40 °C to +125 °C	3000	Reel

[1] SPQ = Standard Pack Quantity.

8.1 Coding rule

Figure 8-1: Coding rule